

Impact of High-Thermal Budget Anneals on Polysilicon as a Micromechanical Material

Yogesh B. Gianchandani, *Member, IEEE*, Meenam Shinn, and Khalil Najafi

Abstract— With the goal of facilitating the development of surface micromachined polysilicon MEMS with *postprocessed* on-chip circuitry, we have evaluated the impact of a 1200 °C 16-h anneal upon chemical-vapor-deposited (CVD) polysilicon under a variety of processing conditions. The results show that undoped polysilicon has a final stress of +10–20 MPa even when the films are vastly different as deposited and that phosphorus doping introduces a compressive trend that is evident only after the long anneal. X-ray diffraction, transmission-electron-microscopy (TEM), and atomic-force-microscopy (AFM) studies of the polysilicon are used to analyze the grain orientations, grain sizes, and surface roughness of the material. The effect of the long anneal on residual stress in wet thermal and CVD oxides is also presented. Overall, the results indicate that the thermal budgets of conservative circuit processes can be accommodated within the fabrication sequence of surface-micromachined polysilicon microstructures. [266]

Index Terms—Actuators, anneal, integrated circuits, polycrystalline silicon, sensors, stress, transducers.

I. INTRODUCTION

THE TRADITIONAL approach to the integration of circuitry with surface-micromachined polysilicon microstructures has been to perform most of the circuit fabrication steps (excluding, perhaps, metallization) before depositing the structural polysilicon at 550–650 °C [1], [2]. Although this approach eliminates concerns about the effect of topological variations of microstructures on subsequent processing steps, it is not without drawbacks. One concern is that polysilicon chemical-vapor deposited (CVD) for thick microstructures may have a thermal budget large enough to impact sensitive circuit parameters, and another is that the usage of unmodified circuit processes available from foundries as modular units is constrained. Such concerns have motivated efforts to reverse the traditional approach by fabricating the microstructures before the circuitry [3]–[5]. In the revised approach, the polysilicon MEMS are recessed into the Si surface, allowing the wafer to be planarized before the circuitry is fabricated. The circuit parameters are thus unaffected by the thermal budget of the microstructure fabrication. Instead,

Manuscript received April 28, 1997; revised September 12, 1997. Subject Editor, E. Obermeier. This work was supported by the Samsung Advanced Institute of Technology and Dr. C.-M. Song of the Samsung Corporation.

Y. B. Gianchandani is with the Department of Electrical and Computer Engineering, University of Wisconsin, Madison, WI 53706-1691 USA (e-mail: yogesh@engr.wisc.edu).

M. Shinn is with the Samsung Advanced Institute of Technology, Suwon, Korea.

K. Najafi is with the Center for Integrated Sensors and Circuits, University of Michigan, Ann Arbor, MI 48109 USA.

Publisher Item Identifier S 1057-7157(98)01300-6.

it becomes critical to assess the impact of the circuit thermal budget upon the structural polysilicon.

Previous reports have described residual stress in polysilicon as a function of deposition conditions, such as temperature and pressure, and as a function of rapid thermal or furnace anneals with relatively low thermal budgets (≤ 1100 °C, ≤ 3 h) [6]–[10]. Wishing to explore the possibility of using circuit processes which have high-thermal budgets, in this investigation we annealed the samples at 1200 °C for 16 h (in N₂) [11]. This anneal was derived from the p-well drive-in step in a conservative 3- μ m complementary metal-oxide-semiconductor (CMOS) process and has a larger thermal budget than most circuit processes require [12]. The impact of the long anneal upon the polysilicon is described for a variety of processing conditions: 1) the effect of the long anneal upon residual stress is evaluated by wafer curvature measurements for polysilicon deposited at two different temperatures. X-ray diffraction, transmission-electron-microscopy (TEM), and atomic-force-microscopy (AFM) studies of the polysilicon films are presented as evidence of the resultant grain orientations, grain dimensions, and surface roughness, respectively; 2) the effect of phosphorus diffusion before the long anneal upon the final residual stress is described; and 3) since CVD and wet thermal oxide are often used in conjunction with polysilicon, the effect of the long anneal upon the residual stress in these films is also evaluated.

II. EXPERIMENTAL RESULTS

In our experiments, the polysilicon was deposited in an LPCVD furnace with a 6-in ϕ tube flowing 80-sccm SiH₄. Two types of polysilicon films were used: 1) at 570 °C and 150 mT, a 1.3- μ m-thick amorphous layer was deposited at a rate of ≈ 30 Å/min. It had a residual stress of about +82 MPa and 2) at 625 °C and 180 mT, a 3- μ m-thick layer was deposited with a grain size of about 1000 Å. The deposition rate of ≈ 100 Å/min provided improved throughput. The residual stress in this layer was –205 MPa. The substrates were 4-in ϕ Si wafers with ≈ 7700 -Å thermal wet oxide grown at 1100 °C. The process variations that were explored and the residual stress data obtained are summarized in Fig. 1.

In branches A and B, the two types of polysilicon were annealed without any intervening doping or RTA steps. The final stress was +10–20 MPa for both. This low tensile value is very suitable for microstructures since it prevents buckling. Fig. 2 shows the X-ray diffraction spectra for annealed samples from branches A and B as well as the unannealed 625 °C polysilicon of branch B. The Bragg peaks are marked with the crystal

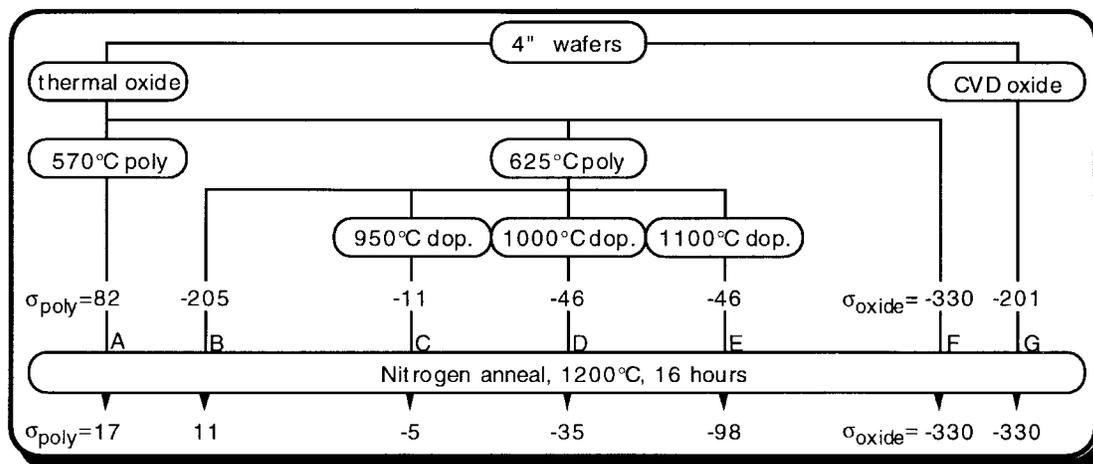


Fig. 1. A flow chart summarizing the experiments and results. Stress values are in MPa.

TABLE I
ROUGHNESS OF THE POLYSILICON SURFACES AS DETERMINED BY AFM OVER A $5 \times 5 \mu\text{m}^2$ AREA

Poly Deposition Temperature	Subjected to Long Anneal?	Peak Roughness (nm)	RMS Roughness (nm)
625°C	No	264	36
625°C	Yes	258	38
570°C	Yes	173	18

orientations that they represent. It should be noted that equal distributions of (111), (220), and (311) grains would generate relative intensities of 100, 60, and 35, respectively. The region from 65° to 75° is blanked out to eliminate the (400) peak of the Si substrate. It is clear that the (111) orientation dominates both branches after the anneal. In contrast, the orientation is almost exclusively (220) for unannealed 625 °C polysilicon, in agreement with [10]. The postanneal grain size as measured by TEM is 2000–4000 Å for both 570 and 625 °C polysilicon (Fig. 3). Since the value reported after a 1100 °C, 30-min anneal is >2000 Å [8], it is plausible that the grain growth slows down or even ceases at some point in the long anneal. The TEM samples were prepared by etching the substrate from the backside, so the image in Fig. 3 is of the upper surface of the polysilicon.

The roughness of the polysilicon surfaces was quantified by tapping mode AFM and is presented in Table I. It is clear that the 625 °C polysilicon is significantly rougher than the 570 °C polysilicon and that its roughness is relatively unaffected by the anneal.

In branches C, D, and E, the 625 °C polysilicon was diffused with phosphorus at 950, 1000, and 1100 °C, respectively. The deposition and soak were each 1 h long, and the dopant source was POCl_3 . The residual stresses before and after the long anneal are plotted in Fig. 4. Sheet resistances, as measured with a four-point probe after the long anneal, are also included. Evidently, a linear relationship evolves between the doping temperature and the residual stress: post anneal compression increases in magnitude by ≈ 30 MPa for every 50 °C rise in doping temperature above 950 °C. This correlation does not exist before the long anneal. It is worth noting that, as expected after the long anneal, SUPREM simulations yield a flat doping profile across the polysilicon in all three samples. Furthermore,

microstructures were patterned from the polysilicon doped at 950 °C and appeared flat upon release. Although quantitative data is not available at this point, this observation suggests that the residual stress profile is also flat.

Wet thermal and CVD oxides were annealed in branches F and G, respectively. The CVD oxide was deposited 2 μm thick at 920 °C and 450 mT using N_2O and SiCl_2H_2 flow rates of 120 and 60 sccm, respectively. The anneal changed the CVD oxide stress from -210 to about -330 MPa, which was the same as the thermal oxide stress before and after the anneal.

All the stress values were calculated from the change in wafer curvature after stripping the deposited thin films from the back of the wafer. (Consequently, all the wafers had bare backs during the long anneal.) Stress calculations require knowledge of film thickness, which was measured using a reflectance spectrometer, an ellipsometer, or both. Uncertainty in the stress values results primarily from measurements of the wafer curvature and film thickness, and is estimated to be about $\pm 10\%$.

III. CONCLUSIONS

A number of specific observations can be made on the basis of the experiments performed.

- 1) After the long anneal, undoped polysilicon is in mild tension ($< +20$ MPa) regardless of the original deposition temperature and the as-deposited residual stress. Furthermore the long anneal transforms the dominant grain orientation to (111). The grain size grows to 2000–4000 Å. Since 625 °C polysilicon has a $3\times$ higher deposition rate than 570 °C polysilicon, these results make a case for using the former as the microstructural material in the interest of increased throughput. The only

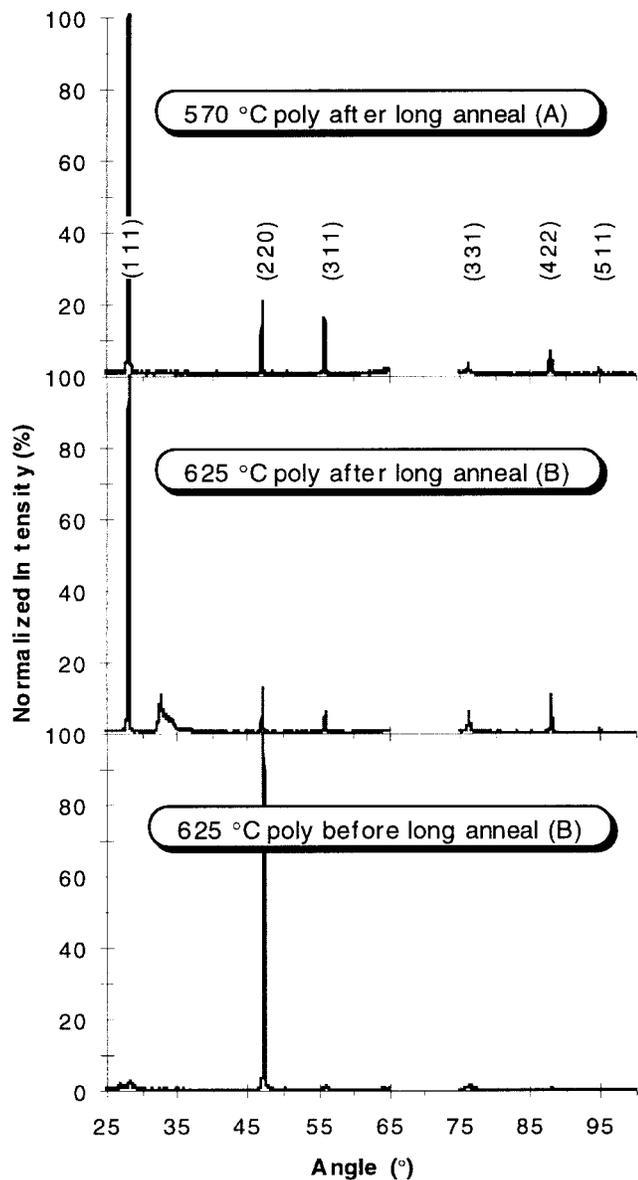


Fig. 2. X-ray diffraction spectra for branches A and B of Fig. 1.

caveat is that the rms roughness of the former, at 36 nm, is twice that of the latter under the deposition conditions that were used. (This, however, could conceivably be improved by changing the deposition pressure.)

- 2) Phosphorus diffusion before the long anneal introduces compressive stress linearly related to the doping temperature. Specifically, a 1-h deposition and 1-h soak at 950, 1000, and 1100 °C causes the final stress to be -5 , -35 , and -98 MPa, respectively. This also implies that the compressive stress is inversely related to the sheet resistance.
- 3) The residual stress of CVD oxide changes from -210 to -330 MPa during the anneal, whereas the stress in wet thermal oxide grown at 1100 °C remains constant at the latter value.

Overall, the results confirm that a long anneal at 1200 °C for 16 h (in N_2), which is representative of the thermal budget of a conservative circuit process, can be accommodated within



Fig. 3. The TEM of 625 °C poly after the long anneal (branch B).

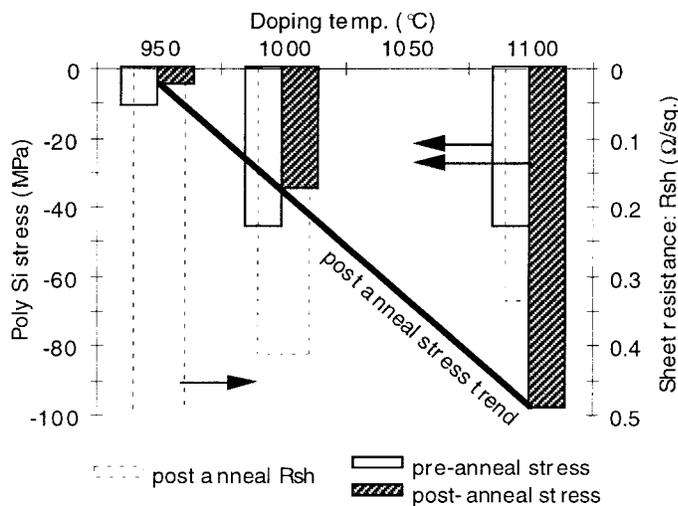


Fig. 4. Stress and R_{sh} versus doping temperature (branches C, D, and E). The postanneal doping concentrations as simulated by SUPREM are: 8.5×10^{16} , 2.9×10^{17} , and $1.9 \times 10^{18} \text{ cm}^{-3}$ for the samples doped at 950, 1000, and 1100 °C, respectively.

the fabrication sequence of surface micromachined polysilicon microstructures.

ACKNOWLEDGMENT

The authors thank Dr. L. J. Parfitt for the X-ray scans, K. Linder for the TEM, and Dr. J. Mansfield and E. Y. Wang for the AFM.

REFERENCES

- [1] R. T. Howe and R. S. Muller, "Resonant-microbridge vapor sensor," *IEEE Trans. Electron Devices*, vol. 33, no. 4, pp. 499–506, 1986.
- [2] W. Kuehnel and S. Sherman, "A surface micromachined silicon accelerometer with on-chip detection circuitry," *Sens. Actuators A*, vol. 45, pp. 7–16, 1994.
- [3] J. H. Smith, S. Montague, J. J. Sniegowski, J. R. Murray, and P. J. McWhorter, "Embedded micromechanical devices for the monolithic integration of MEMS with CMOS," in *Proc. Int. Electron Devices Meet. (IEDM'95)*, Dec. 1995, pp. 609–612.
- [4] J. T. Kung, "Methods for planarization and encapsulation of micromechanical devices in semiconductor processes," U.S. Patent 5 504 026, Apr. 2, 1996.
- [5] M. Offenbergl, F. Larmer, B. Elsner, H. Munzel, and W. Riethmuller, "Novel process for a monolithic integrated accelerometer," in *Proc. Int. Conf. Solid-State Sensors and Actuators (Transducers'95)*, June 1995, pp. 589–592.
- [6] H. Guckel, D. W. Burns, C. C. G. Visser, H. A. C. Tilmans, and D. DeRoo, "Fine grained polysilicon films with built-in tensile strain," *IEEE Trans. Electron Devices*, vol. 35, no. 6, pp. 800–801, 1988.
- [7] P. Krulevitch, R. Howe, G. Johnson, and J. Huang, "Stress in undoped LPCVD polycrystalline silicon," in *Proc. Int. Conf. Solid-State Sensors and Actuators (Transducers'91)*, June 1991, pp. 949–952.
- [8] P. J. French, B. P. van Driehhuizen, D. Poenar, J. F. L. Goosen, R. Mallee, P. M. Sarro, and R. F. Wolffenbuttel, "The development of a low-stress polysilicon process compatible with standard device processing," *IEEE J. Microelectromech. Syst.*, vol. 3, no. 5, pp. 187–196, 1996.
- [9] T. Scheiter, M. Biebl, C. Hierold, and H. Klose, "Rapid thermal annealing of doped silicon films to relax intrinsic stress," *Sens. Mater.*, vol. 8, no. 7, pp. 445–454, 1996.
- [10] X. Zhang, T.-Y. Zhang, M. Wong, and Y. Zohar, "Effects of high-temperature rapid thermal annealing on the residual stress of LPCVD-polysilicon thin films," in *Proc. IEEE Micro Electro Mechanical Syst. (MEMS'97) Workshop*, Jan. 1997, pp. 535–540.
- [11] Y. B. Gianchandani, M. Shinn, and K. Najafi, "Impact of long, high temperature anneals on residual stress in polysilicon," in *Proc. Int. Conf. Solid-State Sensors and Actuators*, Chicago, IL, June 1997, pp. 623–624.
- [12] J. Ji and K. D. Wise, "An implantable CMOS circuit interface for multiplexed microelectrode recording arrays," *IEEE J. Solid-State Circuits*, vol. 27, no. 3, pp. 433–443, 1992.



Yogesh B. Gianchandani (S'83–M'85) received the B.S. degree in 1984 from the University of California, Irvine, the M.S. degree in 1986 from the University of California, Los Angeles, and the Ph.D. degree in 1994 from the University of Michigan, Ann Arbor, all in electrical engineering.

He was with Xerox Corporation from 1985 to 1988 and with Microchip Technology from 1988 to 1989, working in the area of integrated circuit design. From 1994 to August 1997, he was a Research Fellow in the Center for Integrated Sensors and Circuits at the University of Michigan. Since then, he has been with the University of Wisconsin, Madison, as an Assistant Professor in the Department of Electrical and Computer Engineering. His research interests include all aspects of design, fabrication, and packaging of micromachined sensors and actuators and their interface circuits. These include devices and systems with applications in inertial sensing, environmental sensing, scanning microscopy, data storage, and biomedical applications.

Dr. Gianchandani is a Member of Tau Beta Pi and Eta Kappa Nu.



Meenam Shinn received the B.S. and M.S. degrees in materials science and engineering from Hanyang University, Korea, in 1985 and 1988, respectively, and the Ph.D. degree from Northwestern University, Evanston, IL, in 1993.

From 1993 to 1994, she worked as a Postdoctoral Fellow at Northwestern University in the field of thin films. In November 1994, she joined Samsung Advanced Institute of Technology, Korea. Since then, she has been engaged in the research and development of microelectromechanical systems including integrated inertial sensors as a Senior Researcher.

Khalil Najafi (S'84–M'86–SM'97), for a photograph and biography, see this issue, p. 15.