PROGRESS IN SILICON ETCHING BY IN-SITU DC MICROPLASMAS

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ABSTRACT

This paper reports on the etching of Si using spatially confined SF_6 microplasmas that are generated by applying a DC bias across a metal-polyimide-metal electrode stack patterned on a sample substrate. The typical operating pressure and power density are in the range of 1-20 Torr and 1-10 W/cm^2, respectively. The plasma confinement can be varied from <100μm to >1 cm by variations in the electrode area, operating pressure, and power. Etch rates of 4-17 μm/min have been achieved. The etch rate per unit power density increases with increasing pressure, while the plasma resistance decreases with increasing power density. In a shared anode configuration, which is suitable for small feature sizes, reducing the trench width from 106 μm to 6 μm reduces the etch rate by 14%. Numerical modeling is used to correlate variations in the local electric fields to measured trends in the etch rate and asymmetry in the etch profile.

I. INTRODUCTION

Plasma processing is extensively utilized in semiconductor processing applications, and is the dominant silicon etching technique. Silicon etching is commonly performed in parallel plate reactors by applying RF power (typically at 13.56 MHz) between two electrodes placed several centimeters apart. The silicon wafer is located on the powered electrode for reactive ion etching. The operating pressure and power are in the range of 10-500 mTorr and 10-500 mW/cm^2, respectively. Since the plasma exists globally across the wafer, the etch is selectively masked by a thin film of photoresist, SiO_2, or metal which is patterned on the wafer surface. More recently, fast anisotropic etches have been demonstrated by alternative plasma etchers utilizing electron cyclotron resonance (ECR) [1] and inductively coupled plasmas (ICP) [2]. All of these options, however, employ a single plasma that acts over the entire surface area of a wafer. Creating several different etch depths or profiles in a single die mandates the use of a like number of masking steps.

In contrast to traditional techniques, an *in-situ* microplasma is formed by applying DC power between two thin-film metal electrodes patterned on the Si substrate and separated by a dielectric spacer (Fig. 1). First described in [3], this arrangement not only shields the substrate from applied electric fields, but also permits the use of DC power, eliminating the tuning requirements of RF plasmas. The tri-layer stack also serves as the hard mask for etching patterns that are smaller than the confinement limit of the microplasma. The stack is fabricated by a two-mask process. Although conventional methods require only one mask, it is notable that when several different etch depths/profiles are required, the microplasma approach results in net savings because etch parameters of each spatially confined etch region can be individually determined. The relatively small electrode areas for in-situ microplasmas allow power densities in the range of 1-10 W/cm^2 to be achieved at modest levels of input power. The relatively large operating pressures of 1-10 Torr serve to spatially confine the plasmas. Consequently, several microplasmas with different etch characteristics may operate simultaneously or sequentially on different regions of a wafer.

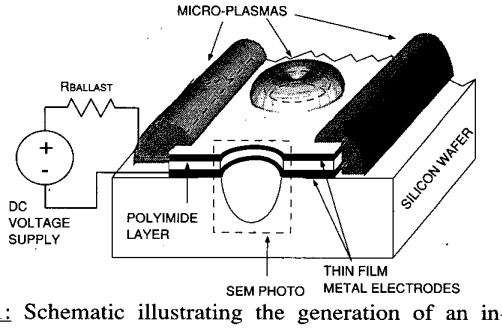

Fig 1: Schematic illustrating the generation of an in-situ microplasma.

II. EXPERIMENTAL RESULTS

Test samples were fabricated from Si wafers using a two-mask process sequence for the electrode stack. The first lithography mask was used to pattern the upper metal layer and the polyimide. The second mask was then used to pattern the lower metal layer and simultaneously re-pattern the upper metal as well. Metal layers that have been investigated include chrome, aluminum, titanium, and nickel. Following the microplasma etch, the electrode stack can be stripped by sacrificing the lower metal electrode in the appropriate wet etchant.

In the electrical set-up, the pads for the two in-situ electrodes are contacted by probes and connected to a DC power supply across a series ballast resistor, which provides a means to control the plasma current. As shown in Fig. 1, the upper electrode serves as the anode, whereas the lower electrode is connected to ground, in order to direct the positive ions in the plasma toward the Si substrate. Typical

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bias values range from 300-600 V, depending on the ambient gas used and target etch rate.

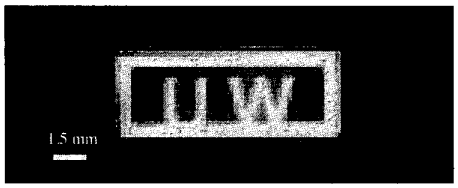

Fig. 2: Local confinement of N_2 microplasmas at 1-20 Torr and -360 V DC.

The spatial self-confinement of microplasmas is shown in Fig. 2 as a glow that is localized to the in-situ electrodes. In this experiment, the ambient gas was N_2, and the bias voltage was -360 V, which has opposite polarity to the bias normally used for etching. By varying the power and pressure the confinement can be changed from <100 μm to >1 cm.

Typical etch profiles achieved by microplasmas are shown in Fig. 3. In each of these cases the etch was performed though openings in the in-situ electrodes using a partial pressure of SF_6. Figure 3(a) shows a 92 μm deep etch through a circular opening of 150 μm diameter, that was achieved in 20 min. at 2.7 Torr, with a power density of 3.2 W/cm^2 averaged over the electrode area. The sidewall angle was 21° off vertical. The electrode metal used in this case was aluminum. Figure 3(b) shows the cross-section of a 207 μm deep etch through a 280 μm wide, 2.2 mm long slit opening. The electrode metal used in this case was titanium. The etch was achieved in 24 min. at 5.2 Torr and 6.8 W/cm^2. The sidewall angle of this etch was nearly vertical in certain locations of the profile. The profiles shown in Fig. 3 indicate that varying degrees of anisotropy can be achieved by changing the operating conditions of microplasmas.

The etch rate of Si in SF_6 microplasmas was studied as a function of several operating parameters. Figure 4 shows the dependence of the etch depth on the duration of the etch. These etches were performed under two sets of conditions: case A used 2.7 Torr pressure, 1.6 W/cm^2 power density, and Al electrodes with circular openings of 350 μm diameter; case B used 5.2 Torr, 6.8 W/cm^2, and titanium electrodes with 280 μm wide slit openings. Case A achieved etch rates of 4-7 μm/min., whereas Case B achieved etch rates of 9-12 μm/min. In both cases the etch rate was significantly higher for the first few minutes, and then rapidly settled at a lower value that was stable for 50 minutes. Although the reasons for the higher initial etch rate remain to be determined, it is noteworthy that the electric field above the exposed Si is highest for the first few minutes of an etch, during the time that the etched depth is relatively small. This is shown as a modeling result in the next section.

Figure 4 also shows that under the conditions of case B, it was possible to etch though a wafer in less than an hour. Through-wafer etches were routinely achieved with the use of titanium electrodes, which developed considerably less damage than aluminum from sputtering in exposed regions of the cathode. This is consistent with trends seen in conventional etchers [4].

In order to evaluate the variation of etch rate with power density, four etches were performed for three minutes at 2.7 Torr using aluminum electrodes with circular openings of 350 μm diameter. The etch rate increased linearly with power from 1.4 μm/min. at 0.73 W/cm^2 to 17.4 μm/min. at 7.4 W/cm^2. Since the etch rate is linearly related to electrode power density, it is worthwhile to evaluate the etch rate per unit power density as a figure of merit for the efficiency of the etch. Figure 5 shows this parameter as a function of chamber pressure for three minute long etches performed though a 280 μm wide slit opening in titanium electrodes. As the pressure was increased, the power necessary to sustain the plasma increased from 3 to 7 W/cm^2. Despite this, the ratio of the etch rate to power density increased from 0.15 to 4.23 μm/min per W/cm^2 as the pressure was changed from 2 to 20 Torr. Higher ratios achieved by other operating parameters are also shown in Fig. 5.

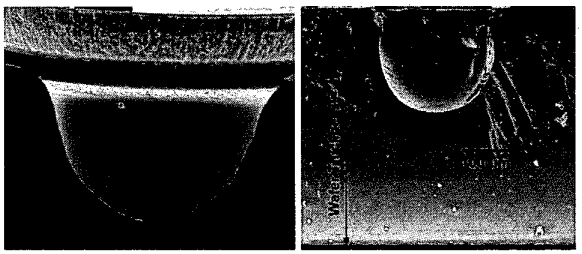

Fig. 3: (a-left) A 92 μm deep etch through a 150 μm ø circular opening (2.7 Torr, 3.2 W/cm^2, 20 min.); (b-right) A 207 μm deep etch through a 280 μm wide slit opening (5.2 Torr, 6.8 W/cm^2, 24 min.).

An alternate arrangement of the electrodes is called the shared anode configuration. In the electrode arrangement of Fig. 1, which is also shown as a cross-section in Fig. 6a, the entire electrode stack assists in masking the protected areas from the local microplasma. However, when the lateral dimensions of the trench are small, it is easier to fabricate an electrode arrangement in which the lower metal serves this purpose alone, resulting in a shared anode arrangement of Fig. 6b. The variation of etch rates with lateral dimensions of the mask opening was explored in the shared anode configuration. The openings were 1.75 mm long and ranged in width from 106 μm to 5.6 μm. The normalized etch rates for a 3 minute etch performed at 7.2 W/cm^2 power density are plotted in Fig. 7. Under these circumstances, the 95% reduction in opening width was monotonically related to a 14% reduction in etch rate.

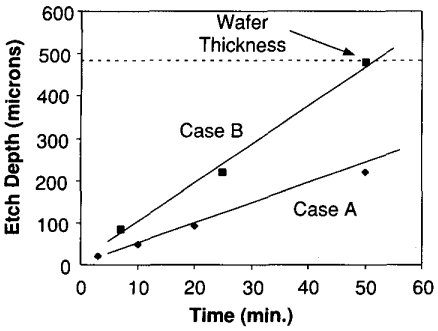

Fig 4 : Etch progression for two cases described in the text. Through-wafer etches can be achieved in <1 hour.

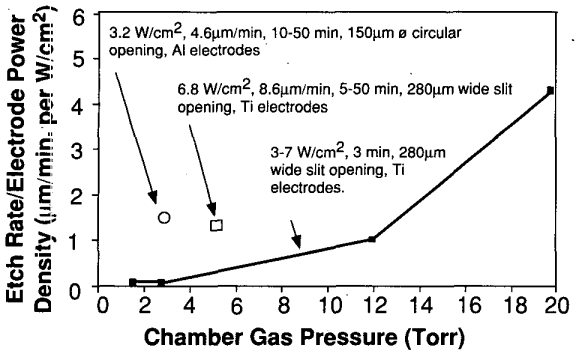

Fig 5: The ratio of the etch rate to the electrode power density increases with chamber pressure.

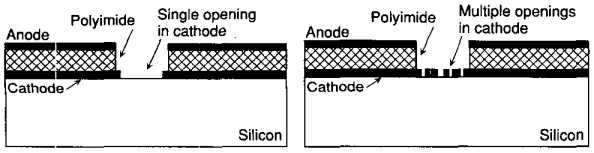

Fig. 6: (a-left): The single cavity configuration of Fig. 1. (b-right): The shared anode configuration.

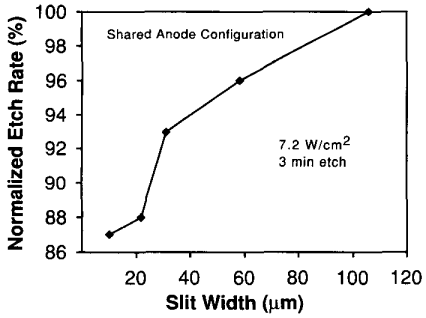

Fig. 7: Normalized etch rate for varying etch widths in the shared anode configuration.

In plasmas having power density that is typically used for semiconductor processing, ion-electron pairs are vastly outnumbered by neutral species [5]. As a consequence, when the applied voltage is increased, the energy increase results in appreciably more electron-neutral collisions than electron-electron collisions. This increases the plasma density, but does not substantially increase the electron temperature. The higher plasma density then results in a larger plasma current, which is observable as a drop in plasma resistance with an increase in the power density. Figure 8 plots the measured resistance of the microplasmas as a function of the power density. The measurements for Fig. 8 were obtained at 2.7 Torr using thin film aluminum electrodes of 0.2 cm^2 area.

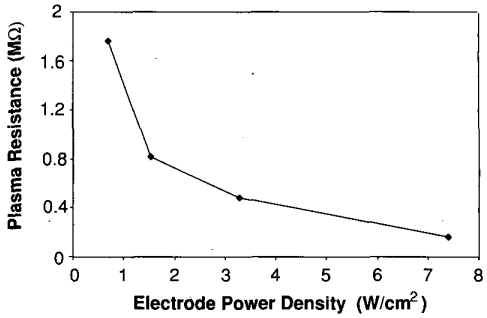

Fig 8: The plasma resistance decreases with power density.

It was observed that minor variations in etch profiles could be correlated to the location of the slit opening within the expanse of the electrode. This concept is illustrated in an exaggerated manner in Fig. 9. The parameter *X* denotes the normalized location of the opening within the width of the electrode, whereas *Y* denotes the normalized location of the nadir of the etch profile within the opening. This, a data point at *X=Y=0.5* would represent a symmetrical etch profile for a opening located in the center of the electrode. Experimental results indicated that in openings that were close to the edges of the electrode, the nadir was skewed toward the outer edge, i.e., the values for *X* and *Y* were proportional to each other, as shown in Fig. 10. This trend was verified for a variety of etch conditions. The measurements also showed that the asymmetry in the etch profile diminished as the etch progressed and the trench became deeper. This phenomenon is thought to be due to an asymmetry in the electric fields that exists for openings for which the value of *X* is close to 0 or 1. It will be discussed further in the next section.

III. MODELING

Under the conditions described in the preceding sections, the etching is believed to be performed by ions which are pulled away from the sheath that exists above the electrode stack by the electric field associated with the openings in the stack. The effect of feature size and location on local electric fields was estimated by using the numerical simulator MAXWELL™. For simplicity, the conductivity and charge distribution of the plasma was neglected. A 30 µm thick polyimide-metal-polyimide electrode stack was assumed to exist on a 500 µm thick silicon wafer. The relative dielectric constant of the polyimide was 3.5, and the resistivity of the metal was zero. The simulations showed

that equipotential contours were crowded closer together in and above narrow openings, indicating that the local electric fields were higher. Conversely, the local electric fields extend to greater heights above the wider gaps in electrodes, indicating a broader reach into the plasma above. The simulations also indicated that the local electric field reduces as an etch progresses and the trench depth exceeds its width (Fig. 11a, b). This is consistent with the observation made in the preceding section that the initial etch rate is higher than the cumulative average rate.

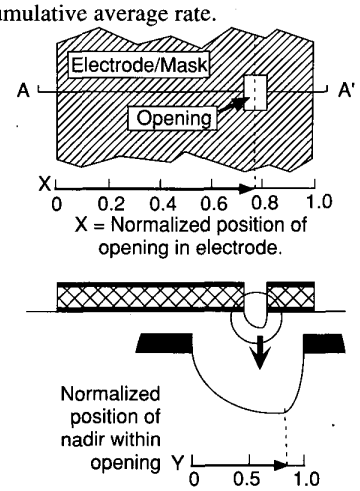

Fig. 9: The asymmetry in an etch profile can be correlated to the location of the slit opening.

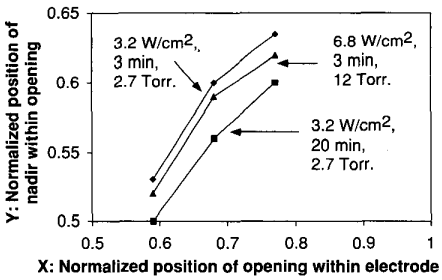

Fig. 10: The nadir of the etch profile is slightly skewed toward the electrode edge when the opening is near the periphery.

Electric field simulations were performed to investigate the correlation between the etch profile and the opening location shown in Fig. 10. The results indicate that the electric field component that is parallel to the sample surface and points toward the edge of the electrode is somewhat larger for openings located close to the periphery. This is evident from a comparison of Fig. 11a with Fig. 11c.

IV. CONCLUSIONS

This effort has demonstrated that Si wafers can be etched by microplasmas that are generated by DC power applied between thin film electrodes patterned on a wafer surface. Etch rates >17 μm/min. and through-wafer etches were achieved using SF_6. The typical operating pressure and power density were in the range of 1-20 Torr and 1-10 W/cm^2, respectively. The etch rate depended linearly on the electrode power density; the power efficiency of the etch rate increased with pressure. In the shared anode configuration, the etch rate of 5 μm wide trenches was 14% lower than that of 106 μm wide trenches. The change of the plasma resistance with the power density was found to comply with theoretical expectations. Certain trends of etch rates and etch profiles were qualitatively correlated to local electric fields created by the thin film electrodes.

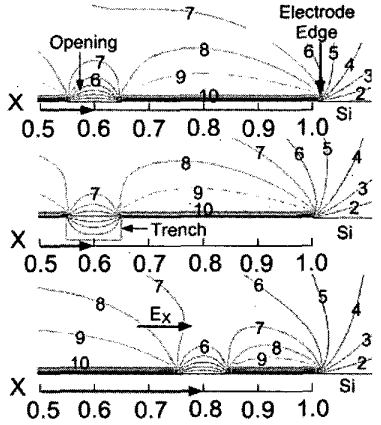

Fig. 11: Simulated equipotential contours: (a-upper) shallow trench close to center of electrode stack; (b-middle) deep trench near center; (c-bottom) shallow trench near edge.

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