ROOM TEMPERATURE DEPOSITION OF SILICON BY ARRAYED DC MICROPLASMAS

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ABSTRACT

This paper reports *room temperature* deposition of silicon in *spatially localized* areas of a micro-chip through plasma-enhanced chemical vapor deposition (PECVD) using micro-plasmas. DC microplasmas are generated on a patterned Ti arrayed electrode structure employing multiple cathodes and a single anode. At the operating pressures used, the plasma glow is confined to the region directly over the powered cathodes only. Powering these microplasmas in a silane ambient allows selected deposition of silicon to only the energized cathodes. Silicon is deposited at 6.7-15.9 nm/min. corresponding to microplasma cathode power densities of 3.65-9.35 W/cm^2, with the substrate heated to 300°C. At room temperature deposition rates up to 7.5 nm/min. are realized. A new plasma coupling technique for creating controlled variations in a sub-array of unbiased electrodes is also described.

I. INTRODUCTION

Plasma Enhanced Chemical Vapor Deposition (PECVD) is one of the most widely used processes to deposit a variety of materials − silicon in particular − onto substrates for MEMS and IC processing. This process allows a uniformly thick material to be deposited over the entire substrate; unwanted material can then be etched off, or removed by a variety of means. A variety of potential applications could require an array of varying thicknesses of silicon: selective trimming of oscillators, or selective deposition of filtering layers for optical or chemical sensors. Selective deposition of thin-film materials has long been recognized as a practical method of reducing mask count in processes which requires this material or structural diversity. In the past, selective CVD has been achieved by localized heating with on-chip heaters [1]. While this is a powerful method, heating with local resistors is not always desirable or possible, and PECVD is more appealing for certain situations. In conventional PECVD, the plasma exists operates at 10-500 mTorr pressure, and 50-200 mW/cm^2 RF power, and the substrate is heated from 300-600 °C. This limits the substrate material choices. For example, post package trimming of MEMS devices can not be done using this process, due to the heat contraints.

Localized *in-situ* etching of Si using DC microplasmas ignited across a metal-polyimide-metal stack patterned on the same wafer has been demonstrated in the past [2]. This effort demonstrates the first use of in-situ microplasmas for deposition. In particular, it focuses on the deposition of thin-film Si in an array using co-planar Ti electrodes on a glass wafer. This arrangement not only shields the substrate from applied electric fields, but also permits the use of DC power, eliminating the tuning requirements of RF plasmas. The relatively small electrode areas for in-situ microplasmas allow power densities in the range of 1-10 W/cm^2. The relatively large operating pressures of 1-6 Torr serve to spatially confine the microplasma to the cathode [3]. This distinction from conventional plasmas is critical to the success of this method.

In addition to previous etching results, and this new deposition work, microplasmas have been the focus of increasing research in recent years. Other efforts have been directed at miniaturizing inductively coupled plasmas to be utilized for gas spectroscopy [4], and to utilize DC microplasmas as an optical emission source for gas chromatography [5]. Efforts have also been made to implement microplasmas into microdisplay systems [6], study the electrostatic breakdown in vacuum-packaged MEMS [7], and to magnetically confine microplasmas [8]. Work has also been done employing the water sample as a cathode, with a metallic anode for detecting water impurities through spectral information [9],[10]. This technology has also been extended to make on-chip UV radiation sources [11].

II. EXPERIMENTAL RESULTS

A critical advantage in utilizing on-chip microplasmas for selective deposition of silicon is the ability to spatially localize the glow of these discharges. When microplasmas are generated between an array of coplanar electrodes, such as that shown in Fig. 1, the glow region of the discharge is confined to the cathode region only.

Spatial self-confinement of a microplasma operating at 430 V in N_2 ambient at 2 Torr is illustrated in Fig. 2. The glow at these operating parameters remains localized to the cathode pixels; un-powered pixels, and the anode pixels sustain no glow. In prior work, it was found that confinement of the glow to the cathode is not a function of anode-cathode spacing. Instead, it is a function of background gas pressure, applied power density, and cathode geometry. Microplasmas are typically formed in a

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background gas ranging from 1–20 Torr, with electrode power densities ranging from 1–100 W/cm^2. As the background pressure is increased, confinement to the cathode is improved; as power densities increase confinement is lessened.

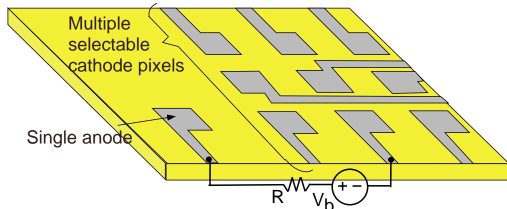

Fig. 1: Microplasmas can be independently generated on electrodes patterned on the wafer substrate. A single anode can be utilized; individual glows are localized above powered pixels.

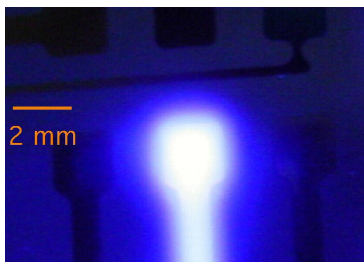

Fig. 2: Microplasmas are confined to the powered cathode only. This image at 2 Torr at 430 V, in N_2.

Silicon deposition results obtained in silane ambient with the configuration shown in Fig. 1 are shown in Figs. 3-6. Figure 3a shows a pixel in the array that was grounded as a cathode, with the corresponding anode powered at 495 V, and an electrode power density of 5.6 W/cm^2. This was performed in a chamber at a 1.2 Torr vacuum with an 100/100 sccm Ar/silane gas flow, with the substrate heated to 300 °C. Figure 3b shows a similar pixel on the array that was left ungrounded, thereby maintaining a floating potential. Silicon deposition could be achieved by grounding those cathode pixels which were to be coated. Figure 4 shows a SEM shot of the silicon deposited on the pixel seen in Fig. 3a.

Fig. 3: (a-left) Powered cathode pixel in an array, after 5 min. of deposition at 1.2 Torr, and 300 °C; (b-right) un-powered cathode pixel from the same array

Fig. 4: SEM photo of silicon deposited on the pixel shown in Fig. 3a.

An array of pixels was fabricated by patterning 1.5 μm thick Ti on a Pyrex glass substrate. The individual pixels were powered for varying durations and power densities. These microplasmas were operated in a 1.7 Torr vacuum, with a 100/100 sccm Ar/Silane gas flow, and the substrate heated to 300°C. Applied power densities ranged from 3.65-9.35 W/cm^2. This array is shown in Fig. 5. It can be seen that two pixels, A and B that were never powered did not have have any deposited silicon. The anode was discolored from heat, but had no silicon deposition. Figure 6 shows the maximum silicon thickness formed on each pixel. As is reasonable, the thickest silicon was generated on the pixel with either the longest deposition period (pixel D, 20 min. at 3.65 W/cm^2) or the highest power density (pixel F, 5 min. at 9.35 W/cm^2).

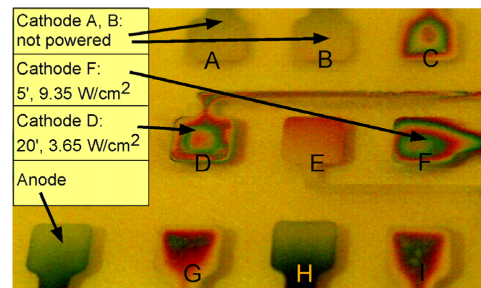

Fig. 5: Individually addressed pixel array with deposited silicon, 300 °C, at 1.7 Torr, for varying power densities and times, in a silane ambient.

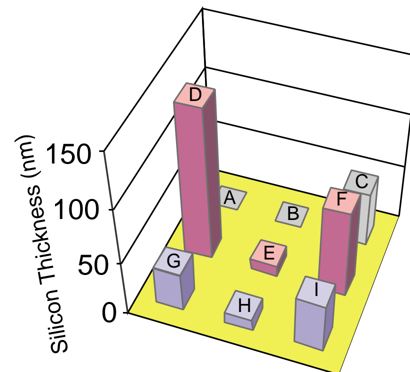

Fig. 6: Maximum silicon thickness per pixel on the array of Fig. 3.

Figure 7 shows silicon deposition rates and their variation with applied power density. The rates vary from 6.7-15.9 nm/min. for the explored power densities which are comparable to conventional PECVD. The deposition rate is

quite linear with power density, and is not found to be a function of anode-cathode spacing. Figure 8 shows the deposition rate as a function of applied power density, substrate temperature, and deposition duration. Two specific points merit discussion. First, in all cases deposition rates are highest in the beginning, slowing down after time. Second, microplasmas provided deposition of silicon on selected cathode pixels at *room temperature*. At similar power densities, room temperature deposition occurs at about one-third the 300°C deposition rate. This allows an appreciable silicon deposition rate on a host of MEMS materials unable to withstand high temperatures.

A peel test was performed by affixing tape to the silicon, and removing it, as well as by dicing through the individual pixels. All tests found no delamination or peeling of the deposited silicon.

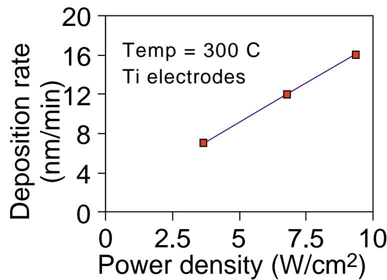

Fig. 7: Deposition rate of silicon is very linear with applied power, and is not a strong function of anode-cathode spacing.

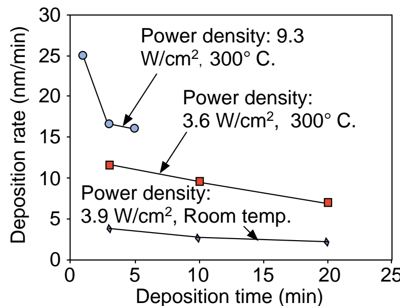

Fig. 8: Silicon deposition rates vs. time for varying power densities and temperatures at 1.7 Torr, 100/100 sccm Silane/Ar gas flow.

III. PLASMA COUPLING

The power delivered to an array of floating pixels can be controlled by utilizing a microplasma itself as a variable resistor. A floating pixel cathode couples to an adjacent powered one in certain regimes of input power and operating pressure as the microplasma varies in confinement. Figure 9 shows a pictograph of the array, with a cutaway schematic view, illustrating a simple equivalent circuit for the plasma coupling. The pads have an associated capacitance to ground. The microplasmas also have an associated breakdown voltage, modeled as a zener diode to the powered anode. The resistors allow leakage of charge to neighboring floating pixels. This leakage current causes the capacitors to charge up and permits the plasma to ignite over a floating pixel. As the diode thresholds and the leakage resistance are functions of the pressure, power cathode geometry and spacing, proximate pixels can be turned on or off without leads. This permits significantly higher density arrays, and simplifies powering schemes.

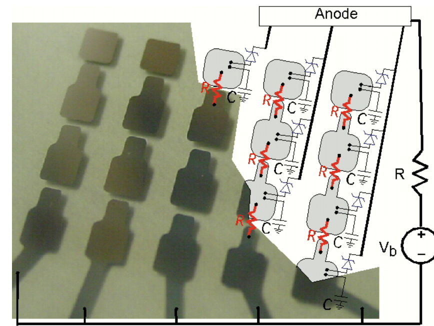

Fig. 9: Microplasmas couple to proximate floating electrodes in an array. The level of coupling is determined by electrode spacing, operating power and pressure. The equivalent electrical circuit due to the plasma is shown in the cutout.

Figure 10 shows two on-chip floating electrodes proximate to a powered cathode in N_2. As microplasmas are more confined to the cathode at higher pressures, the resultant leakage resistance decreases at pressure decreases. The pixels in Fig. 10 vary in distance from the powered electrode, with edge to edge spacings of 300 and 1000 µm, respectively. Figures 10(a) and (b) show this configuration operating at 4 and 2 Torr, respectively. It can be seen in Fig. 10(b) that the change in pressure lowers coupling resistance, powering the closest pixel.

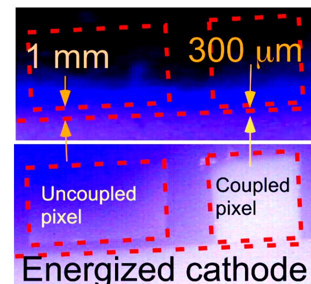

Fig. 10: Floating but un-powered electrodes proximate to N_2 microplasma at 4 Torr (a-upper); and powered at 2 Torr, illustrating varying plasma coupling (b-lower).

Figure 11 shows an array of floating pixels fabricated from titanium patterned on a glass substrate. Room temperature silicon deposition was performed on this array by powering the electrodes with leads (electrodes A-E) with differing voltages and power densities. Pixels A through E were powered consecutively and at different operating pressures. In all cases gas flow was 100/100 sccm silane/Ar, and pressure was varied from 1.4-2.1 Torr; operating voltages were varied from 420-650 V, DC. Plasma from the powered

electrodes successfully coupled to the floating electrodes (pixels F-T). Variations in the pixel to pixel spacing and the dimensions of the tab extending from the pixel, as well as the operating pressure and power densities correspond to different coupling resistances. Room temperature deposition, in four steps, resulted in a controlled 5X4 array of silicon, varying from 0-141 nm (Fig. 12). The silicon deposited on pixels A,F,K, and P was a result of pixel A being powered at 5.2 W/cm^2, at 2.1 Torr, for 18 min. In comparison, the silicon deposited on pixels B,G,L, and Q was by powering pixel B at 3.2 W/cm^2, at 1.4 Torr, for 9 min. The rate of silicon deposition increases at higher operating pressures, however, plasma coupling to neighboring pixels correspondingly decreases. The silicon deposited on pixels C,H,M, and R was by pixel C being powered at 4.9 W/cm^2, at 1.7 Torr, for 15 min. Pixels D,I,N, and S had silicon deposited with the same operating conditions, but for 12 min.

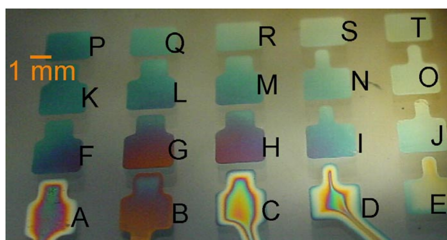

Fig. 11: Silicon selectively deposited on a floating array structure. Deposition was performed at room temperature, under varying pressures and times.

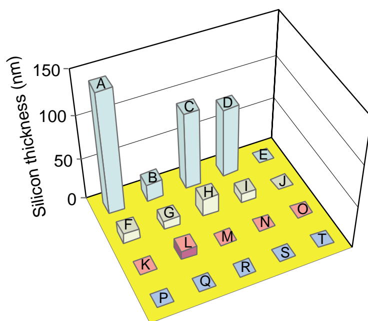

Fig. 12: Silicon thickness per pixel on floating array. Pixel coupling is greatest at 1.4 Torr. Deposition rate is highest at 2.1 Torr. All depositions at room temperature.

V. CONCLUSIONS

Microplasmas were generated with thin-film Ti arrays patterned on glass substrates by selectively powering individual cathode pixels. When the microplasmas were formed, the glow was confined to the region over the cathode only. In a silane ambient, the microplasmas were used to locally deposit silicon selectively on the powered cathodes. With a substrate temperature of 300°C, deposition rates ranging from 6.7-15.9 nm/min. were measured. At *room temperature,* deposition rates of up to 7.5 nm/min were realized. In addition to a controlled method of producing arrays of varying silicon thickness, this process allows deposition of silicon on materials that will be damaged by the higher temperature conventional PECVD process. Silicon of 20 different thicknesses ranging from 0-141 nm was deposited on a densely packed 5X4 electrode array, in a four step process. Fifteen pixels in the array were unbiased. Microplasmas, the confinement of which can be controlled by pressure, power density, and electrode geometry, form power-coupling leads to neighboring pixels. This allows a controlled array of varying thicknesses of silicon to be deposited on-chip, with a simplified powering scheme, at room temperature.

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