Selective Deposition of Silicon at Room Temperature Using DC Microplasmas

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***Abstract*—This paper reports deposition of silicon at elevated and room temperatures in spatially localized areas of a microchip by plasma-enhanced chemical vapor deposition using microplasmas. The microplasmas are generated by providing dc power to thin-film Ti electrodes patterned on the microchip. Electrode arrangements include configurations in which multiple cathode elements share a single anode. At the operating pressures used, the plasma glow is confined to the region directly over the energized cathodes only, and the deposition is localized to these regions. A silane ambient allows Si to be deposited at 6.7–15.9 nm/min using cathode power densities of 3.65–9.35 W/cm^2, with the substrate heated to 300 °C. At room temperature, deposition rates up to 4.2 nm/min are realized. Also described is a plasma-coupling technique that permits isolated metal pads to be powered by plasma spreading from a proximate cathode at certain levels of power and pressure. This permits controlled variations of silicon thickness in a subarray of unbiased electrodes, simplifying the powering scheme.**

***Index Terms*—Plasma-enhanced chemical vapor deposition (PECVD), polysilicon, thin-film deposition.**

I. Introduction

THE PROGRESSIVE reduction in feature sizes used for modern integrated circuits has placed increasing emphasis on processing methods that minimize the thermal budget to control diffusion and thermal damage in recent years. As a consequence, plasma-enhanced chemical vapor deposition (PECVD) has evolved into one of the most widely used processes to deposit a variety of materials (silicon in particular) onto substrates for microelectromechanical system (MEMS) and integrated circuit processing. This process allows a uniformly thick material to be deposited over the entire substrate; unwanted material can then be etched off, or removed by a variety of means. However, a number of potential applications would benefit from the ability to vary the deposited thickness across an array of features. These include, for example, selective trimming of micromachined oscillators, or selective deposition of filtering layers for optical or chemical sensors. Selective deposition of thin-film materials has long been recognized as a practical method of reducing mask count in processes that requires this material or structural diversity. In the past, selective CVD has been achieved by localized heating with on-chip heaters [1]. Although this is a powerful method, heating with local resistors is not always desirable or possible, and PECVD is more appealing for certain situations.

In conventional PECVD of silicon films, the plasma operates at 10–500 mtorr pressure and 50–200 mW/cm^2 RF power, whereas the substrate is heated to 300 °C–600 °C [2]. Lower temperature PECVD recipes for silicon nitride (175 °C) and silicon dioxide (225 °C) are available [3], [4], but these temperatures are still too high for certain applications, such as the potential post-package trimming of MEMS devices. Room temperature PECVD of amorphous silicon has been reported in recent years [5], [6], but like conventional PECVD, it is not spatially localized. The work described here focuses on localized PECVD using thin-film electrodes patterned on the microchip itself. In addition to room temperature operation, it has other features, described below, that can be beneficial in certain contexts.

It has been demonstrated in the past that localized *in situ* etching of Si can be performed using dc microplasmas ignited across a metal–polyimide–metal stack patterned on the same wafer [7]. It was shown that at operating pressures of 1–20 torr and power density of 1–10 W/cm^2, Si etch rates of 4–17 μm/min could be achieved in an SF_6 ambient. In contrast, this effort[1] demonstrates the first use of *in situ* microplasmas for deposition. In particular, it focuses on the deposition of thin-film Si in an array using side-by-side planar Ti electrodes on a glass wafer. This arrangement not only shields the substrate from applied electric fields, but also permits the use of dc power, eliminating the tuning requirements of RF plasmas. The relatively small electrode areas needed for *in situ* microplasmas allow power densities in the range of 1–10 W/cm^2 to be achieved with relative ease. Additionally, the relatively large operating pressures of 1–6 torr serve to spatially confine the microplasma to the cathode [9]. These distinctions from conventional plasmas allow maskless localized silicon deposition of a variety of thicknesses. This paper also describes a plasma-coupling technique that permits isolated metal pads to be powered by plasma spreading from a proximate cathode at certain levels of power and pressure.

In addition to previous etching results and this new deposition work, microplasmas have been the focus of increasing research in recent years. Other efforts have been directed at miniaturizing inductively coupled plasmas to be utilized for gas

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[1]Portions of this paper have appeared in conference abstract form in [8].

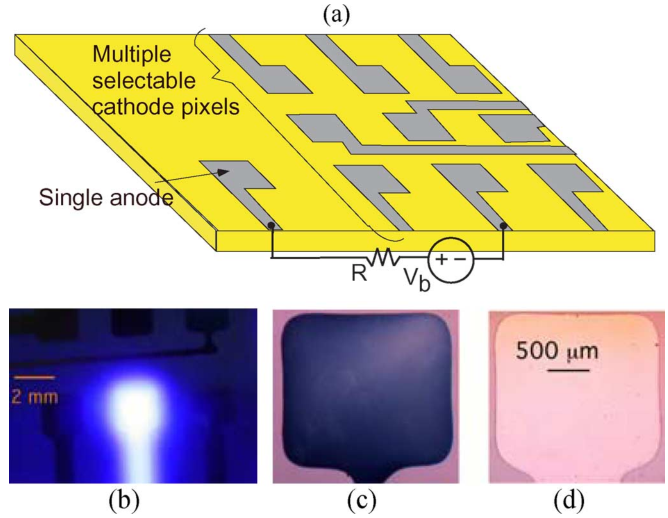

Fig. 1. Microplasmas can be independently generated on electrodes patterned on the wafer substrate. (a) Single anode serving multiple cathode pixels. (b) Localized glow on a cathode pixel at 2 torr and 430 V, in N_2. (c) Powered cathode pixel in an array after 5 min of deposition at 1.2 torr and 300 °C. (d) Unpowered cathode pixel from the same array showing no deposition.

spectroscopy [10] and using dc microplasmas for spectroscopic detection in conjunction with gas chromatography [11]. Efforts have also been made to utilize microplasmas in display systems [12] to study electrostatic breakdown in vacuum-packaged MEMS [13] and to magnetically confine microplasmas [14]. Work has also been done, employing a water sample as a cathode, for detecting water impurities through spectral information [15], [16]. This technology has also been extended to make on-chip UV radiation sources [17].

II. Device Configuration

In the first part of this effort, a planar electrode array was fabricated by patterning a 1.5-μm-thick layer of Ti on a no. 7740 Pyrex glass wafer. A 3×3 array of cathode elements, each 2×2 mm^2 in area, was formed in the vicinity of a single anode element [Fig. 1(a)]. A 2×2 mm^2 patterned anode was used, spaced 6 mm from the outermost pixels. Plasma power was supplied by dc voltage source connected between the anode and the selected cathode. The voltage across a series ballast resistor was monitored to determine the current flow, and from that, the power density was calculated. (A modified array with floating elements and controlled spacings of cathode pixels is described in Section IV.)

As noted previously, a critical advantage in utilizing on-chip microplasmas for selective deposition of silicon is the ability to spatially localize the glow of these discharges. When microplasmas are generated by a pair of coplanar electrodes, such as that shown in Fig. 1, the glow region of the discharge is confined to the cathode region only. Microplasmas that are locally generated and can have power densities controllably tuned can selectively deposit silicon to controlled thicknesses.

III. Experimental Results

The spatial self-confinement of a microplasma operating at 430 V in N_2 ambient at 2 torr is illustrated in Fig. 1(b).

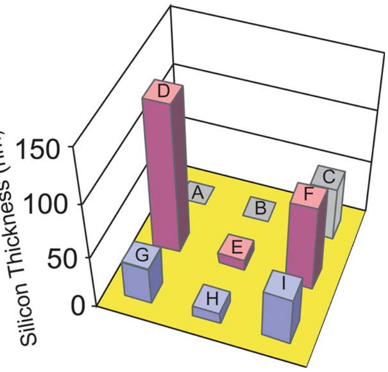

Fig. 2. Maximum silicon thickness per pixel on the array of Fig. 1(a).

The glow at these operating parameters remains localized to the cathode pixels; unpowered pixels and anode pixels sustain no glow. Confinement of the glow to the cathode is not a function of anode–cathode spacing. Instead, it is a function of background gas pressure, applied power density, and cathode geometry. Consequently, multiple cathodes can be powered from the same anode in a controllable fashion. Microplasmas are typically formed in a background gas at pressures ranging from 1 to 20 torr, with electrode power densities ranging from 1 to 100 W/cm^2. As the background pressure is increased, confinement to the cathode is improved; as power densities increase, confinement is lessened.

Silicon deposition results obtained in silane ambient with the configuration shown in Fig. 1(a) are shown in Fig. 1(b)–(d). Fig. 1(c) shows a 2×2 mm^2 pixel in the array that was grounded as a cathode, with the corresponding anode powered at 495 V. The locally generated microplasma corresponded to an electrode power density of 5.6 W/cm^2. This experiment was performed in a chamber at a 1.2-torr vacuum with a 100/100 sccm argon/silane gas flow and the substrate heated to 300 °C. Fig. 1(d) shows a similar pixel on the array that was left ungrounded, thereby maintaining a floating potential. Silicon deposition could be achieved by grounding those cathode pixels that were to be coated with silicon.

The cathode pixels located in a 3×3 array were powered for varying durations and power densities. These microplasmas were operated in a 1.7-torr vacuum, with a 100/100 sccm argon/silane gas flow and the substrate heated to 300 °C. Applied power densities ranged from 3.65 to 9.35 W/cm^2. Fig. 2 shows the maximum silicon thickness formed on each pixel ranged from 0 to 119 nm, depending on the duration and magnitude of power supplied to it. Pixels that were never powered did not have any silicon coating. The thickest silicon was generated on the pixel with either the longest deposition period (pixel D, 20 min at 3.65 W/cm^2), or the highest power density (pixel F, 5 min at 9.35 W/cm^2).

The silicon deposition rates and their variation with applied power density were measured. The rates vary from 6.7 to 15.9 nm/min for power densities ranging from 3.2 to 8.9 W/cm^2. These rates are comparable to conventional PECVD and reveal linear dependence on the cathode power density. In general, deposition rates were not found to be a strong function of anode–cathode spacing: two pixels powered at 3.2 W/cm^2 for 10 min, with respective anode–cathode

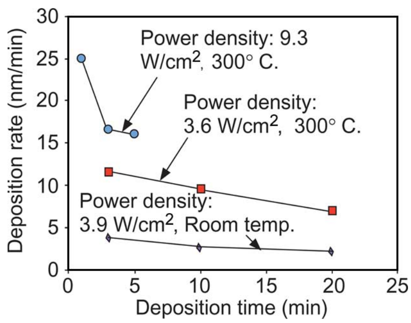

Fig. 3. Silicon deposition rates versus time for varying power densities and temperatures at 1.7 torr and 100/100 sccm silane/argon gas flow.

spacings of 2 and 10 mm, were found to vary only 6% in the maximum silicon thickness. Fig. 3 shows the deposition rate vs. time duration for various applied power densities and substrate temperatures. When the substrate is heated to 300 °C with a cathode power density of 9.3 W/cm^2, deposition rates start at 25 nm/min in the first minute, tapering to 16 nm/min in 5 min. At the same temperature, with a cathode power density of 3.6 W/cm^2, deposition rates start at 12 nm/min, evolving to 7.3 nm/min. At similar power densities, room temperature deposition occurs at about one-third the 300 °C deposition rate, ranging from 4.2 to 2.6 nm/min. This allows an appreciable silicon deposition rate on a host of materials relevant to MEMS unable to withstand high temperatures.

A peel test was performed by affixing tape to the silicon, and removing it, as well as by dicing through the individual pixels. All tests found no delamination or peeling of the deposited silicon.

IV. Plasma Coupling

As indicated previously, the plasma tends to spread away from a powered cathode element as the ambient pressure is decreased or the power density is increased. Since the plasma has some conductance, as it spreads, it can be used to deliver power to an element that is otherwise electrically floating. Thus, the power delivered to an array of floating pixels can be controlled by utilizing the microplasma itself as a variable resistor. A floating cathode pixel couples to an adjacent powered one in certain regimes of input power and operating pressure as the microplasma varies in confinement to the powered cathode. Fig. 4 shows an image of the electrode array that was used in this experiment, along with a cutaway schematic view, illustrating a simple equivalent circuit for this plasma coupling. The patterned pixels have an associated capacitance to ground. The microplasmas have an associated breakdown voltage at which the microplasmas are initiated. This is represented as a Zener diode to the powered anode. The microplasmas also have an associated resistance, which allows leakage of charge to neighboring floating pixels. This leakage current causes the capacitors to charge up and permits the plasma to ignite over a floating pixel. As the diode thresholds and the leakage resistance are functions of the pressure, powered cathode geometry, and spacing, proximate pixels can be turned on or off without patterned leads. This permits significantly higher density arrays and greatly simplifies powering schemes.

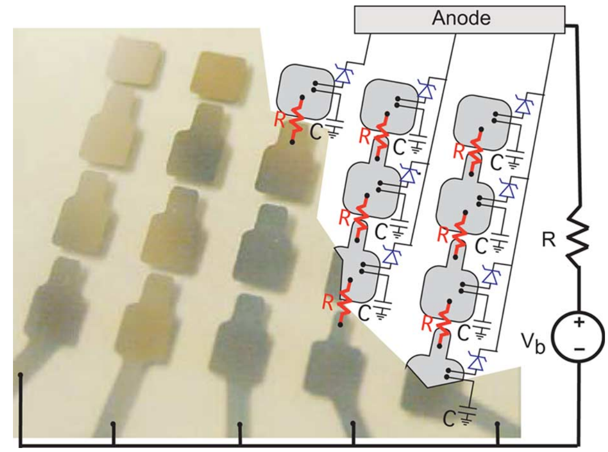

Fig. 4. Microplasmas couple to proximate floating electrodes in an array. The level of coupling is determined by electrode spacing, operating power, and pressure. The equivalent electrical circuit due to the plasma is shown in the cutout.

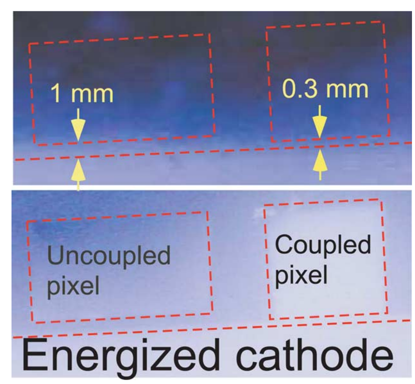

Fig. 5. Floating electrodes proximate to a cathode in N_2 microplasma at 4 torr (above) and 2 torr (below), demonstrating how pixels close to the cathode can be selectively targeted for deposition.

Fig. 5 shows two on-chip floating electrodes proximate to a powered cathode in an N_2 environment. As microplasmas are more confined to the cathode at higher pressures, the resultant leakage resistance decreases as pressure decreases. The pixels in Fig. 5 vary in distance from the powered electrode, with edge-to-edge spacings of 300 and 1000 μm, respectively. The upper and lower parts of this figure show this configuration operating at 4 and 2 torr, respectively. The pixels that are "on" generate plasma and visibly glow purple to pink. It is evident in the lower image that the change in pressure, which lowers the coupling resistance, results in the powering of the closest pixel.

Fig. 6 shows the operating power density of the biased powering electrode and ambient pressure that allows floating pixels to generate microplasmas (be turned on). In an N_2 ambient, the floating pixels can be turned on at pressures ranging from 1 to 5 torr if the proximate biased cathode is provided with a 1.9–6.2 W/cm^2 power density.

Room-temperature silicon deposition was performed on a 5×4 array of titanium pixels patterned on a glass substrate (Fig. 4) by directly powering four of the perimeter cathode pixels in the array with differing voltages and power densities,

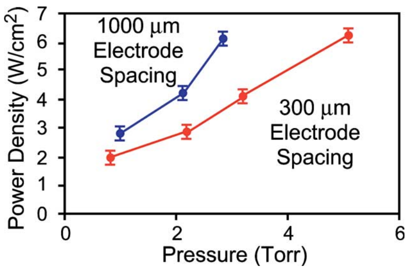

Fig. 6. Power densities and pressures that allow plasma coupling for two different spacings between a powered and a floating electrode. Higher power densities are required for plasma coupling as electrode spacing is increased and as ambient pressure is increased.

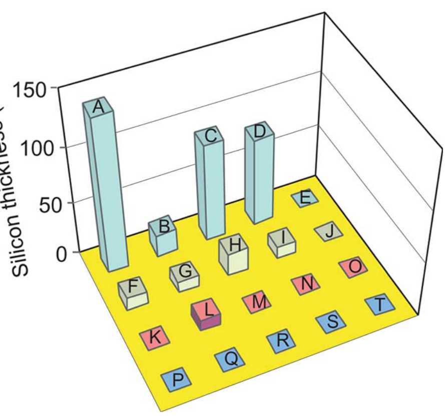

Fig. 7. Silicon thickness per pixel on floating array. Pixel coupling is greatest at 1.4 torr. Deposition rate is highest at 2.1 torr. All depositions were performed at room temperature.

one at a time, at different ambient operating pressures. Fig. 7 labels the cathode pixels, which were each $\approx 2 \times 2$ mm^2 in size; pixels A, B, C, and D were the ones that received direct powering. A 2×10 mm^2 anode was located 3 mm away from the row of pixels P–T. In all cases, gas flow was 100/100 sccm silane/argon, and pressure was varied from 1.4 to 2.1 torr; operating voltages were varied from 420 to 650 V, dc. Plasma from the powered electrodes successfully coupled to the floating electrodes (pixels F–T). Occasionally, some discoloration would be produced in-between cathode pixels, but this was easily removed with a clean wipe. Variations in the pixel-to-pixel spacing and the dimensions of the tab extending from the pixel, as well as the operating pressure and power densities correspond to different coupling resistances. Room temperature deposition, in four steps, resulted in a controlled 5×4 array of silicon, varying from 0 to 141 nm (Fig. 7). The silicon deposited on pixels A, F, K, and P was a result of pixel A being powered at 5.2 W/cm^2, at 2.1 torr, for 18 min. In comparison, the silicon deposited on pixels B, G, L, and Q was by powering pixel B at 3.2 W/cm^2, at 1.4 torr, for 9 min. The rate of silicon deposition increased at higher operating pressures. However, plasma coupling to neighboring pixels correspondingly decreased. The silicon deposited on pixels C, H, M, and R was by pixel C being powered at 4.9 W/cm^2, at 1.7 torr, for 15 min. Pixels I, N, and S had silicon deposition due to the powering of pixel D at 4.9 W/cm^2, at 1.7 torr, for 12 min.

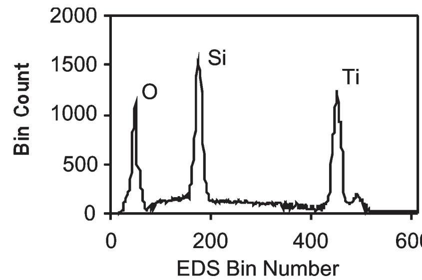

Fig. 8. EDS elemental analysis of pixel G in Fig. 7, detecting Ti (electrode material), Si, and O.

An elemental analysis of the silicon deposited on several pixels was performed using energy-dispersive X-ray spectroscopy (EDS) to verify composition. The data from pixel G in Fig. 7 are shown in Fig 8. Titanium from the cathode pixel and deposited silicon are evident, as well as oxygen, which is probably from the underlying glass structure.

V. Conclusion

Microplasmas were generated with thin-film Ti arrays patterned on glass substrates by selectively powering individual cathode pixels and a single anode structure. When the microplasmas were formed, the glow region was confined to the region over the cathode only. In a silane ambient, the microplasmas were used to locally deposit silicon selectively on the powered cathodes, whereas the unpowered pixels were uncoated. With a substrate temperature of 300 °C, deposition rates ranging from 6.7 to 15.9 nm/min were measured. At room temperature, deposition rates of up to 4.2 nm/min were realized. In addition to a controlled method of producing arrays of varying silicon thickness, this process allows deposition of silicon on materials that will be damaged by the higher temperature conventional PECVD process.

It was also demonstrated that microplasmas, the confinement of which can be controlled by pressure, power density, and electrode geometry, form power-coupling leads to neighboring pixels. This allows neighboring chains of pixels to be turned on or off selectively by controlling the ambient pressure. In particular, for coupling plasma across a 300-μm electrode spacing, as the power density increases from about 3 to about 6.5 W/cm^2, the maximum pressure that can be accommodated increases from about 2.2 to 5 torr. In contrast, to assure coupling across a 1000-μm electrode spacing over the same range of power density, the maximum pressure varies only from about 0.9 to 2.7 torr. Consequently, a controlled array of varying thicknesses of silicon can be deposited on-chip, with a simplified powering scheme, at room temperature. Silicon of different thicknesses ranging from 0 to 141 nm was deposited on a densely packed 5×4 cathode pixel array, in a four-step process in which one perimeter pixel was directly powered in each step.

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