A FABRICATION PROCESS WITH HIGH THERMAL ISOLATION AND VACUUM SEALED LEAD TRANSFER FOR GAS REACTORS AND SAMPLING MICROSYSTEMS

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ABSTRACT

This paper describes a six-mask fabrication process for vacuum-sealed microsystems including pressure and flow sensors, reaction chambers and reservoirs, and channels ranging from 100 nm to 10 μm in hydraulic diameter. All structures are countersunk into a glass substrate, resulting in a planar upper surface that eliminates stress concentrations and also facilitates further lithographic processing. The material choices and structural arrangements are designed to provide high thermal isolation (~$2x10^5$ K/W). Lead transfer between the three available levels of interconnect are accomplished with minimal parasitic capacitance (<1 fF), and low resistance (~1 Ω). A variety of test structures have been successfully fabricated.

I. INTRODUCTION

In recent years there has been substantial interest in developing gas-handling microsystems that can serve as reactors, combustors, and detectors such as mass spectrometers [1-3]. These systems, which may also integrate pumps, reservoirs, flow sensors, and pressure sensors, often operate at elevated temperatures and require high thermal isolation for energy efficiency and minimization of cross-talk. In addition, when capacitive transducers are used, a vacuum-sealed lead transfer with low parasitic capacitance is a significant asset. While there have been strong efforts on vacuum micropackaging [4] and sealed lead transfer [5], research has not been directed at simultaneously achieving high thermal isolation and sub-femtofarad parasitic capacitance.

One common approach to sealing a cavity is to bond a glass or silicon wafer to the top of the substrate. This lid can be a problem for wire-bonding. A method to alleviate this is to use a dissolved wafer process, commonly implemented with a heavily boron doped etch stop in a sacrificial silicon wafer. Unfortunately, the heavily boron doped lid contributes significantly to low thermal isolation and high parasitic capacitance. Furthermore, the highly non-planar resulting structure makes any further processing (such as metallization) difficult. What is necessary is a process to create vacuum-encapsulated devices with high thermal isolation, low parasitic capacitance, and a planar surface both during fabrication and after fabrication (for wire-bonding) to get a high yield.

This paper describes a 6-mask process that accomplishes the three goals of high thermal isolation, low parasitic capacitance lead transfer, and a planar surface during and after fabrication. A variety of proof-of-principle devices were fabricated with this process, including a capacitive-sense pressure sensor, a flow-sensor, and several different sizes of microfluidic channels.

II. DESIGN AND FABRICATION

Figure 1 is a schematic representation of many of the different features of the process that has been developed. A glass substrate is used to increase thermal isolation and minimize parasitic capacitances. Deep channels and cavities are etched in this substrate, and the vacuum-sealed devices are situated within it. There are three levels of interconnect available: a top metal level, a suspended polysilicon level, and a buried metal level. A three-layer dielectric stack separates the top metal level and the suspended polysilicon level. The suspended polysilicon level and the buried metal layers are separated by an air gap. A dielectric cover is anodically bonded to the glass substrate with the use of a polysilicon pad. The dielectric cover is selected to maximize thermal isolation, provide a cover with a small gas permeation rate, and to minimize parasitic capacitances. In addition, the dielectric cover is planar, which not only improves its robustness by eliminating stress concentrations, but also eases the challenges to lithography in subsequent lithography that might be potentially added to the basic sequence.

High thermal isolation is achieved by using a glass substrate, using a cover consisting of silicon dioxide and silicon nitride, and by suspending the hot elements from the cover in a cavity. Polysilicon is not used as part of the cover because of its relatively high thermal conductivity. The distance between a suspended hot element and the edge of the cavity has a large impact on the thermal isolation. However, by using a large gap, high thermal isolation can be achieved.

The polysilicon layer serves many purposes. First, it serves as the bonding pad between the dielectric stack and the glass substrate. Second, it can serve as a deformable cover, such as the diaphragm of a pressure sensor. Third, the polysilicon may be used as a high-temperature heating element. Fourth, it can be an interconnect material. In this process the polysilicon is deposited in two layers of different thickness which are patterned separately. The thinner of these two layers can serve as a spacer for making channels with very small hydraulic diameters (<100 nm), whereas the thicker one can be used for lead transfer between the top metal and buried metal layers.

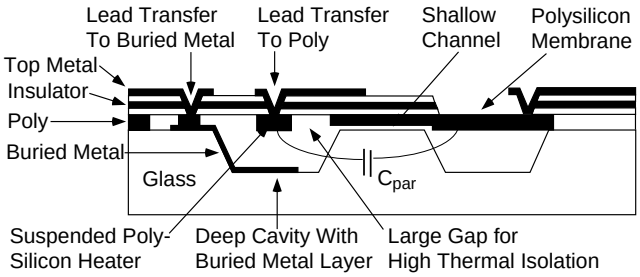

Fig. 1: Cross-section showing some of the features that the presented process provides.

The parasitic capacitance associated with the lead transfer is dominated by the capacitance between the leads involved and the polysilicon closest to them that is used as a bonding pad (C_{par}). Neglecting fringing effects, the lateral capacitance of a polygon that has 1 μm thickness, 160 μm perimeter length and 10-30 μm lateral gap to the surrounding bonding pad, is 140-30 aF.

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With these dimensions the fringing capacitance is expected to be larger, but the overall capacitance is still sub-femtofarad.

The bonding pads formed in the upper metal layer for external lead transfer are suspended on the dielectric cap layer by locally removing the underlying polysilicon. This minimizes the parasitic capacitance associated with them by eliminating all electrically conductive materials from the vicinity of the lead. The suspended bonding pad floats above the glass substrate by the thickness of the polysilicon layer that was etched away (~1 μm), but as will be shown, it is robust enough to be easily tested at a probe station.

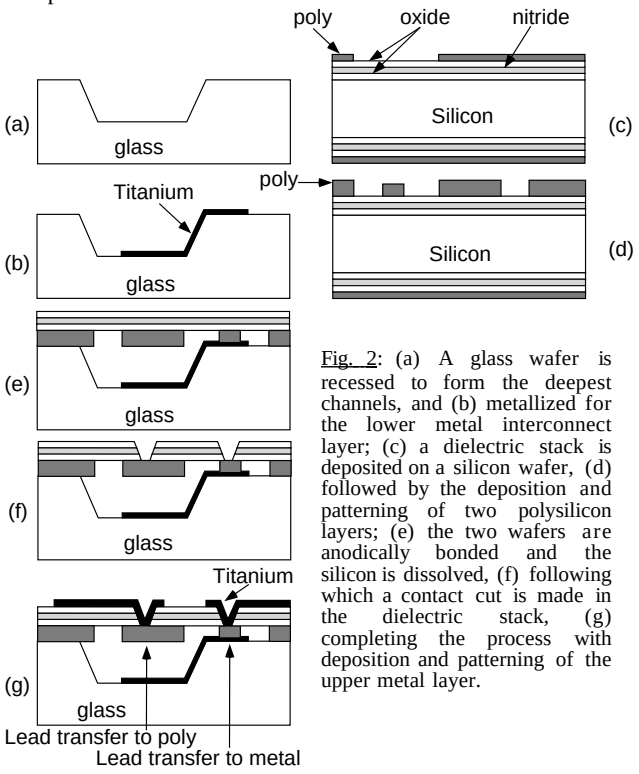

Fig. 2: (a) A glass wafer is recessed to form the deepest channels, and (b) metallized for the lower metal interconnect layer; (c) a dielectric stack is deposited on a silicon wafer, (d) followed by the deposition and patterning of two polysilicon layers; (e) the two wafers are anodically bonded and the silicon is dissolved, (f) following which a contact cut is made in the dielectric stack, (g) completing the process with deposition and patterning of the upper metal layer.

The process starts with bare silicon and Borofloat® glass wafers (Fig. 2). A Cr/Au mask is evaporated onto a clean glass wafer and patterned for wet etch in $HF/HNO_3/H_2O$ 7:3:10 (Fig. 2a). Titanium is then sputtered and patterned on the glass wafer to form the buried metal layer (Fig. 2b). The metal must be about 20 nm thicker than the intended thickness of the thinner of the two polysilicon layers so as to ensure proper mating of the wafers during a later bonding step and also permit lead transfer between the lower metal and the thicker polysilicon layer. The silicon wafer has LPCVD SiO_2, Si_3N_4, SiO_2 (700-400-700 nm) and a thin layer of polysilicon (100 nm) deposited on it. The thin layer of polysilicon is patterned to define the shallow microfluidic channels and recesses for making interconnect between the polysilicon layer and the buried metal layer (Fig. 2c). A thick layer of polysilicon (900 nm) is then deposited, doped, and annealed. In this case the doping is performed in a furnace using POCl, and resulted in a sheet resistance of 8.2 Ω/square for the total 1 μm thickness of the polysilicon. The combined layers of polysilicon are patterned to form the polysilicon heaters, anodic bonding surfaces, polysilicon interconnects, and polysilicon membranes (Fig. 2d). The glass and silicon wafers are then anodically bonded under a vacuum ambient, creating the sealed reservoirs and microfluidic channels. Note that the shallow channels must be shaped such that the rigidity of the wafers in the bonding step is adequate to prevent the channels from sealing shut at this point. The layers on the back of the silicon wafer are removed, and the silicon wafer is dissolved in KOH (Fig. 2e). The dielectric stack is selectively etched to create vias for the top metal to polysilicon interconnect and to create polysilicon membranes (Fig. 2f). Finally, titanium is deposited and patterned to create the top level of interconnect (Fig. 2g).

III. EXPERIMENTAL RESULTS

A variety of test structures and devices were fabricated to serve as a proof-of-concept for this process. The test structures included those for measuring contact resistance between the different interconnect layers and parasitic capacitance of the lead transfer. Structures to measure the thermal isolation were also included. Devices such as Pirani-type flow meters and capacitive pressure sensors were included with shallow and deep channels of 100 nm and 10 μm hydraulic diameters, respectively.

Figure 3 shows a photograph and an SEM of a test device with deep microfluidic channels, reservoirs, shallow microfluidic channels, and pressure sensors. There is less detail shown in the SEM image because much of the structure is encapsulated under a transparent dielectric layer, blocking the electrons, but allowing light through. In the photograph, the pressure sensor membranes and suspended bonding pads are deflected due to the pressure difference between the ambient atmosphere and the vacuum-sealed cavities, but they appear flat in the SEM because of the equalized vacuum ambient.

Figure 4 shows SEM cross-sections of the deep and shallow channels. The deep channel is approximately 10 μm deep, and the shallow channel is less than 100 nm deep. The deep channel has a sloping sidewall favorable for the continuity of a metal lead from the upper surface of the glass to the bottom of the deep channels.

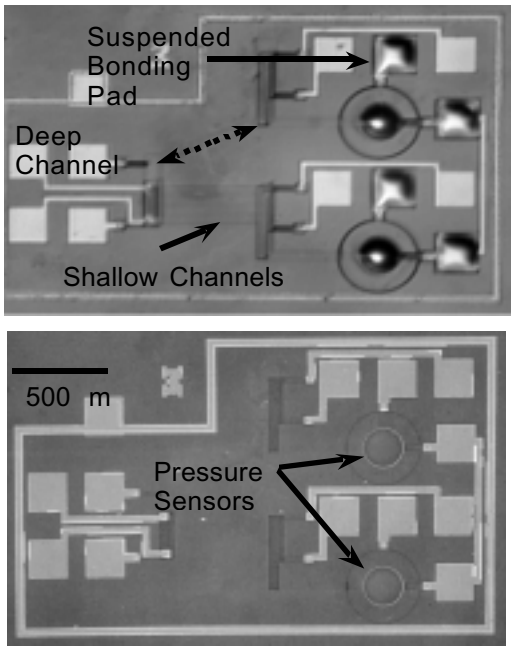

Fig. 3: Photograph (upper) and SEM (lower) of a vacuum encapsulated test structure containing pressure sensors, shallow and deep channels, top and buried metal layers, suspended polysilicon heaters, and lead transfer from the top metal to the polysilicon layer and to the buried metal layer.

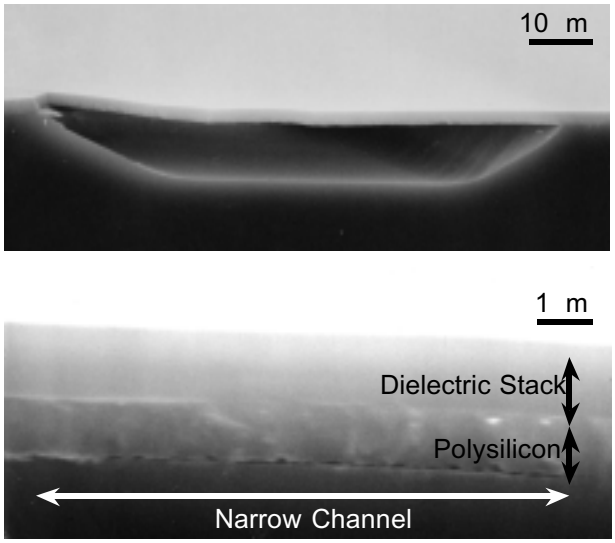

Fig. 4: An SEM of a deep channel (upper) and shallow channel (lower). The height of the shallow channel is only 100 nm, two orders of magnitude smaller than the height of the deep channel.

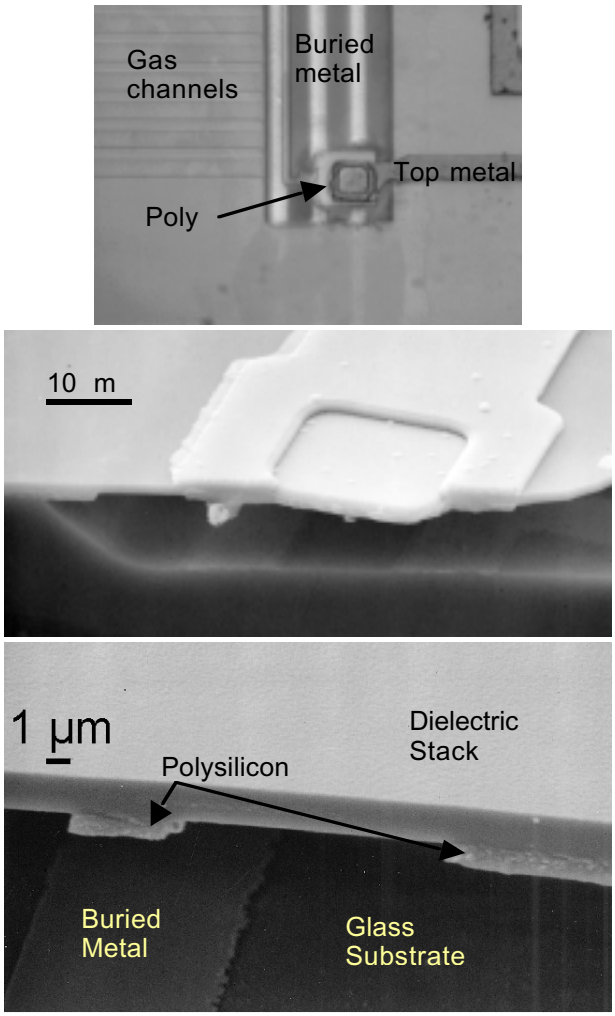

Fig. 5: (a-upper) Optical micrograph of a lead transfer; (b-center) SEM of a suspended lead-transfer from the top metal to a polysilicon layer. (c-lower) SEM of a deep channel showing the buried metal and suspended polysilicon layers.

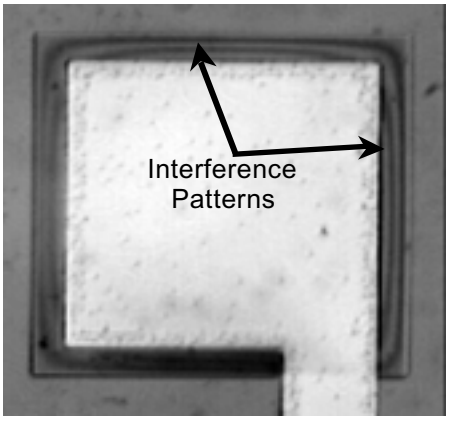

Fig. 6: Photograph of a suspended bonding pad. Interference lines can be seen between the metal and the bonding polysilicon due to the deflection of the pad due to atmospheric pressure.

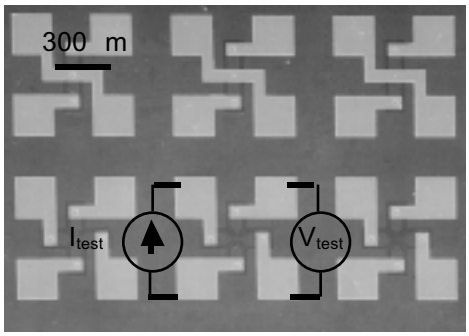

Fig. 7: SEM of six test structures used to measure contact resistance between the various layers. The circuit illustrates the proper connection for a 4-wire resistance measurement.

Figure 5 shows an SEM cross-section of a lead-transfer between the top metal and a suspended polysilicon layer. Below this suspended polysilicon layer can be seen some isolated buried metal layers.

Figure 6 is a photograph of a low-parasitic capacitance suspended bonding pad. There are interference lines visible between the top metal and the polysilicon due to the deflection of the suspended membrane in an atmospheric pressure ambient.

The lead transfer resistance was obtained by using a Kelvin structure, shown in Fig. 7. The contact measurements were made using an Agilent 34401A Multimeter in its 4-wire resistance measurement mode. The electrical connections between the multimeter and the test structure under test are superimposed on Fig. 7. This setup permits measurement of the desired contact resistance independent of any other contact resistances required to get to the desired interconnect layer. The measured lead transfer resistance from the top metal through the polysilicon layer to the buried metal was found to vary between 0.7 Ω and 1.4 Ω for contact areas of 20 μm x 20 μm.

The parasitic lead transfer capacitance was measured between the lead transfer structure and the polysilicon anodic bonding layer using an HP 4284A High-Precision LCR Meter. One probe was connected to the polysilicon bonding layer, and the other probe was positioned above the lead-transfer structure to be tested (Fig. 8a). The LCR meter was zeroed and the capacitance measured as the probe was lowered. Because of the extremely low parasitic capacitance, the capacitance between the probe and the polysilicon bonding layer dominated over the lead-transfer capacitance. The measured capacitance as a function of probe tip height is given in Fig. 8b. As can be seen,

there is no significant increase in capacitance when the probe tip makes contact with the lead-transfer structure, showing that the lead-transfer structure has a capacitance less than 1 fF.

The resistance of a polysilicon heater was found as a function of temperature to obtain the temperature coefficient of resistance (TCR). Measured results are shown in Fig. 9. A current was then passed through a suspended polysilicon heater while the substrate was maintained at room temperature. Both the voltage and current were measured to obtain the power dissipated and the temperature (based upon the measured TCR). Figure 10 shows a plot of the measured dissipated power as a function of temperature. The thermal resistance was found to be $2x10^5$ K/W at the lower end of the tested range. At temperatures higher than about 300°C it decreased by about 10x assuming that the TCR measurement (which as taken over 20-110°C) is valid in this regime.

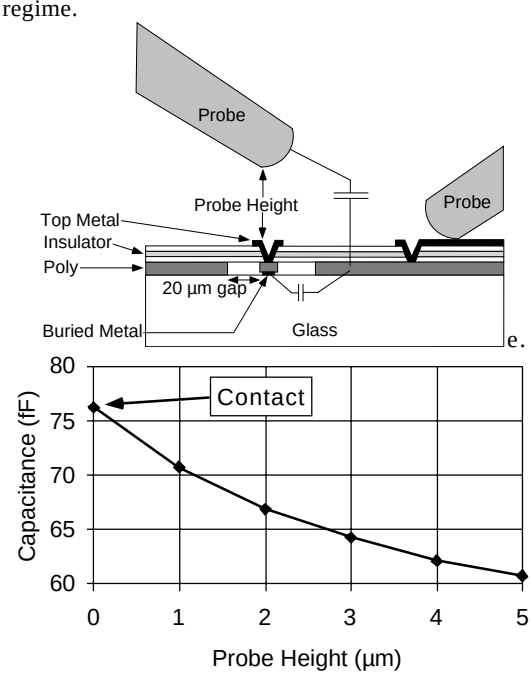

Fig. 8: (a-upper) Parasitic capacitance test set-up. (b-lower) Measured capacitance between a test probe and the bonding polysilicon as a function of the probe height above a lead-transfer structure.

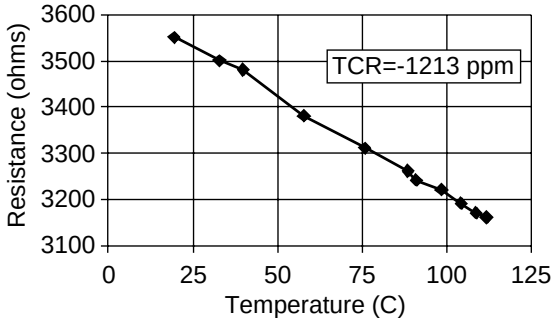

Fig. 9: Plot of resistance versus temperature of a polysilicon heater. The TCR is –1213 ppm.

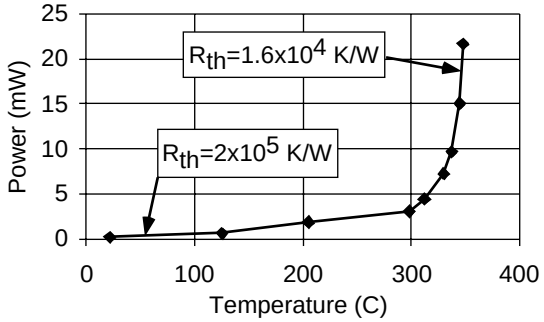

Fig. 10: Power required to heat a 1mm long suspended polysilicon heater to a given temperature, assuming that the TCR measurement of Fig. 9 is valid over the entire rarnge.

IV. CONCLUSION

A six-mask process for microfluidic gas handling systems has been presented that achieves high thermal isolation and very small parasitic capacitance with vacuum sealed lead transfer. It accommodates a variety of elements such as pressure and flow sensors, bolometers, and microfluidic channels of hydraulic diameters ranging from 100 nm to 10 µm or more. High thermal isolation is obtained by using polysilicon heaters suspended on a dielectric membrane with a glass substrate. The measured thermal resistance varied from $2x10^5$ K/W to $1.6x10^4$ K/W, depending upon the temperature. The parasitic capacitance of the lead-transfer structure is found to be less than 1 fF, making this process ideally suited for fabricating capacitive pick-off devices. The resistance of the contacts was found to vary from 0.7 Ω to 1.4 Ω from the top metal through the polysilicon layer to the buried metal. The process can be easily extended to include additional processing steps to create more complicated devices because the resulting structure is highly planar.

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