IMPACT OF LONG, HIGH TEMPERATURE ANNEALS ON RESIDUAL STRESS IN POLYSILICON

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ABSTRACT

This work is intended to facilitate the development of surface micromachined polysilicon MEMS with *post-processed* on-chip circuitry. It evaluates the impact of a 1200°C, 16 hour anneal upon the residual stress in CVD polysilicon under 6 different sets of processing conditions. It shows that (i) undoped polysilicon has a final stress of 10-20 MPa even though the films are vastly different as deposited; (ii) an RTA step at 1000°C before the long anneal increases the final tension to ≈300 MPa; and (iii) phosphorous doping introduces a compressive trend that is evident only after the long anneal. TEM and X-ray diffraction studies of the polysilicon are also presented, as is the effect of the long anneal on wet thermal and CVD oxides.

Keywords: polysilicon, stress, anneal

INTRODUCTION

The traditional approach to the integration of circuitry with surface micromachined polysilicon microstructures has been to perform most of the circuit fabrication steps (excluding perhaps metallization) before depositing the structural polysilicon at 550-650°C [1, 2]. Although this approach obviates concerns for the effect of topological variation of the microstructures on the circuit lithography, the thermal budget associated with the longer polysilicon deposition times required for thick microstructures can impact sensitive circuit parameters. This inflexibility, as well as the attractiveness of using unmodified circuit processes from foundries as modular units motivate efforts to reverse the traditional approach by fabricating the microstructures before the circuitry [3]. The polysilicon MEMS are located between layers of sacrificial oxide in recesses created on the Si surface, allowing the wafer to be planarized before the circuitry is fabricated. The circuit parameters are thus unaffected by the thermal budget of the microstructure fabrication. Instead, it becomes critical to assess the impact of the circuit thermal budget upon the polysilicon.

Previous reports have described residual stress in polysilicon as a function of deposition conditions such as temperature and pressure, and as a function of RTA or furnace anneals with relatively low thermal budgets (≤1100°C, ≤3 hrs.) [4-8]. Wishing to explore the possibility of using circuit processes which have high thermal budgets, in this investigation we annealed the samples at 1200°C for 16 hours (in N_2). Derived from the p-well drive-in step in a conservative 3 μm CMOS process, this anneal has a larger thermal budget than most circuit processes require.

EXPERIMENTAL RESULTS

In our experiments the polysilicon was deposited in an LPCVD furnace with a 6" ø tube flowing 80 sccm SiH_4. Two types of polysilicon films were used: (i) At 570°C and 150 mT, a 1.3 μm thick fine-grain layer was deposited at a rate of ≈30 Å/min. It had a residual stress of about 82 MPa. (ii) At 625°C and 180 mT, a 3 μm thick layer was deposited with larger grain size. The deposition rate of ≈100 Å/min. provided improved throughput. The residual stress in this layer was -205 MPa. The substrates were 4" ø Si wafers with ≈7700 Å thermal wet oxide grown at 1100°C. The experiments are summarized in Fig. 1.

In branches A and B the two types of polysilicon were annealed without any intervening doping or RTA steps. The final stress was 10-20 MPa for both. This low tensile value is very suitable for microstructures since it prevents buckling. Bragg peaks in the X-ray diffraction spectra taken after the long anneal show that the (111) peak strongly dominates in both cases (Fig. 2). In contrast, the (220) peak has been reported as dominant for unannealed polysilicon deposited at 620°C [8]. The post-anneal grain size was measured using TEM at 2000-3000 Å for 570°C polysilicon (Fig. 3), which is comparable to that reported after a 30 min. long 1100°C anneal in [6]. Evidently, the grains do not grow much during the long anneal.

In branches C, D, and E, the 625°C polysilicon was diffused with phosphorous at 950°C, 1000°C, and 1100°C, respectively. The deposition and soak were each one hour long, and the dopant source was $POCl_3$. The residual stresses before and after the long anneal are plotted in Fig. 4. Sheet resistances, as measured with a 4-point probe after the long anneal, are also included. Evidently, a linear relationship evolves between the doping temperature and the stress during the long anneal.

In branch F the undoped 625°C polysilicon was subjected to a series of RTA steps before the long anneal. The RTA was

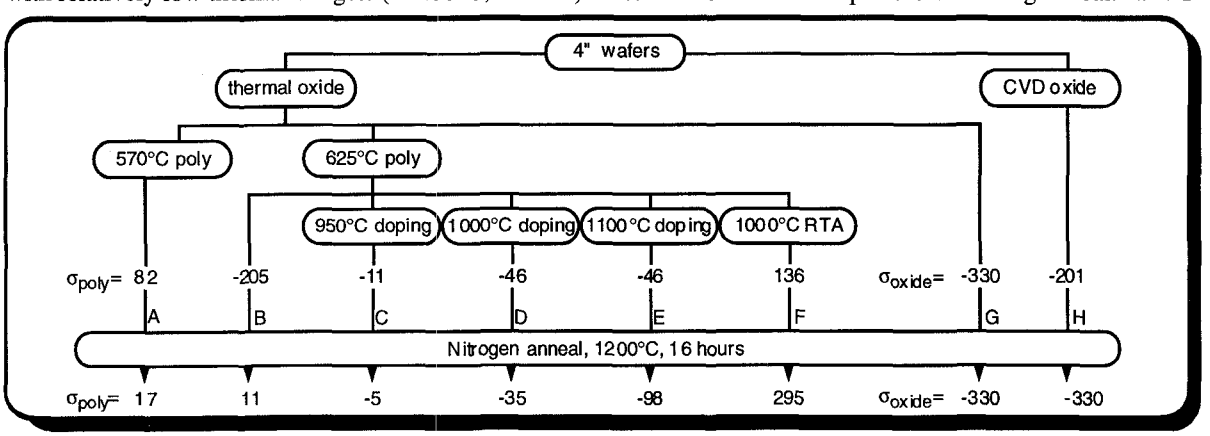

Fig. 1: A flow chart summarizing the experiments and results. Stress values are in MPa.

performed in nitrogen with a 10 sec. soak at 550°C followed by a 5 sec. ramp to 1000°C, where it was held for the stated duration of each cycle. Four 10 sec. cycles were performed, followed by eight 30 sec. cycles and one 60 sec. cycle. The stress evolution of this sample is plotted in Fig. 5. Repeated RTA is equivalent, in this respect, to a single RTA of total duration 5 min. and 40 sec. at 1000°C [8]. The net change in residual stress was from -205 MPa to 136 MPa. The long anneal further increased tension in the polysilicon to 295 MPa.

In branches G and H, wet thermal and CVD oxides were annealed, respectively. The CVD oxide was deposited 2 μm thick at 920°C and 450 mT, using a N_20 and $SiCl_2H_2$ flow rates of 120 sccm and 60 sccm respectively. The anneal changed the CVD oxide stress from -210 MPa to about -330 MPa, which was the same as the thermal oxide stress before and after the anneal.

All the stress values were calculated from the change in wafer curvature after stripping the deposited thin films from the back of the wafer. (Consequently, all the annealed wafers had bare backs.) Stress calculations require knowledge of film thickness, which was measured using a reflectance spectrometer, an ellipsometer, or both. Uncertainty in the stress values results primarily from measurements of the wafer curvature and film thickness, and is estimated to be about ±10%.

CONCLUSIONS

Facing a dearth of published data on the topic, we have subjected polysilicon processed under various conditions to an anneal at 1200°C for 16 hours (in N_2), which is representative of the thermal budgets of conservative circuit processes. Overall, the results indicate that this material is suitable for MEMS. After the anneal undoped polysilicon is in mild tension (<20 MPa) with a dominant grain orientation of (111) regardless of the original deposition temperature. The grain size is 2000-3000 Å. These facts suggest that 625°C polysilicon may be preferable to 570°C because it has a 3X higher deposition rate. Phosphorous doping before the anneal introduces a compressive component linearly related to the doping temperature. For example, doping at 950°C causes the final stress to be -5 MPa. High tension (≈300 MPa) can be achieved in undoped polysilicon by performing RTA before the long anneal. In addition, the experiments show that the residual stress of CVD oxide changes from -210 MPa to -330 MPa during the anneal, whereas the stress in wet thermal oxide remains constant at the latter value.

ACKNOWLEDGEMENTS

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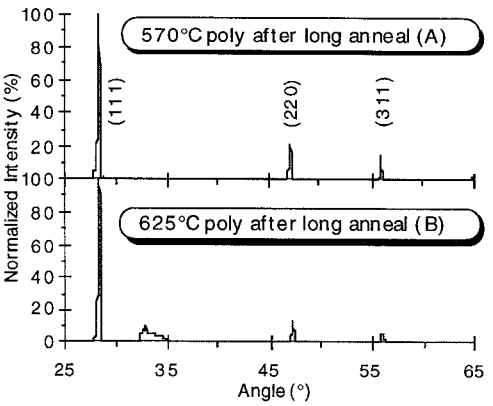

Fig. 2: X-ray diffraction spectra for branches A and B of Fig. 1.

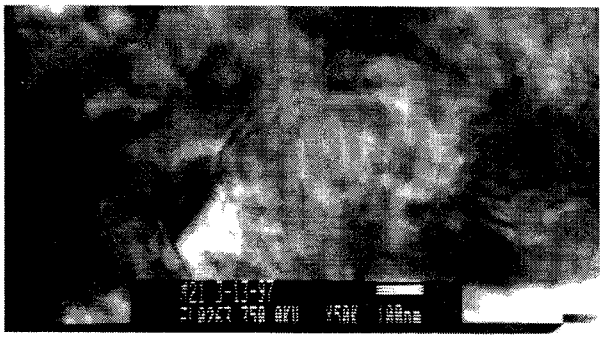

Fig. 3: TEM of 570°C poly after the long anneal (A).

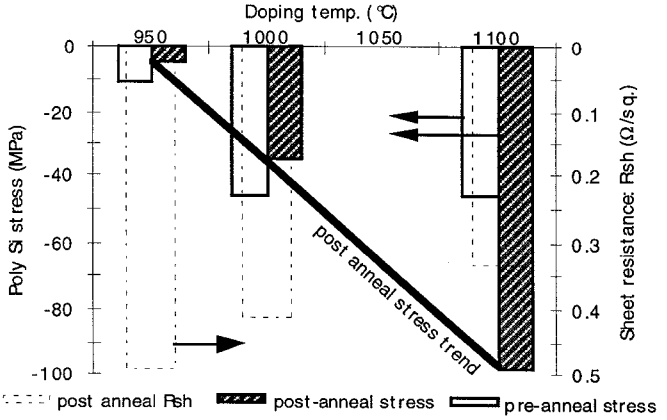

Fig. 4: Stress and R_{sh} versus doping temperature (C, D, E).

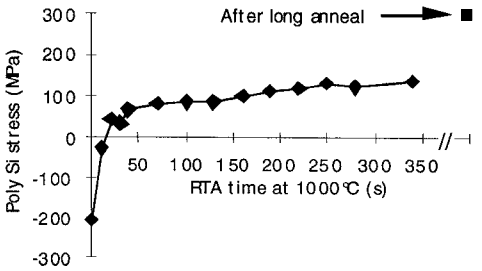

Fig. 5: Stress evolution of 625°C polysilicon with RTA (F).